Bob Dildine, W6SFH

2321 Sycamore Ave, Santa Rosa, CA 95404 **w6sfh@sonic.net**

Buck Converter Basics

Learn how switching power supplies perform their unique "magic."

Several years ago I was asked to come out of retirement and take over the design of several high efficiency switching power supplies. I had almost no experience with switchers and considered them to be mysterious and full of black magic. But after getting my feet wet and working with them for a while, the mystique faded and I realized they were based on a few simple concepts that I hope to share here.

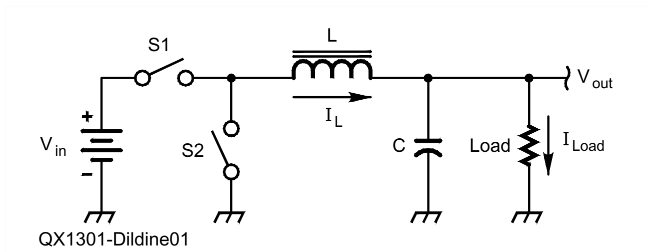

Figure 1 — A basic buck converter.

How It Works

In case you are unfamiliar with the term, a buck converter is a step-down dc-to-dc converter. Let's see how the converter works using the diagram shown in Figure 1.

When switch S1 closes, current flows through the inductor and into the load, charging the inductor by increasing its magnetic field and increasing V_{out}. When V_{out} reaches the desired value, we open S1 and close S2. Current continues to flow in the inductor as the magnetic field collapses and the inductor discharges. Before the inductor completely discharges, we open S2 and close S1 and the cycle repeats. We can adjust the ratio of V_{out} to V_{in} by varying the duty cycle of S1. The longer S1 is turned on, the greater V_{out} will be. The duty cycle of S1 is usually called the converter's duty cycle. If the switches and the inductor are lossless, V_{in} is converted to V_{out} with no loss of power and the conversion is 100% efficient.

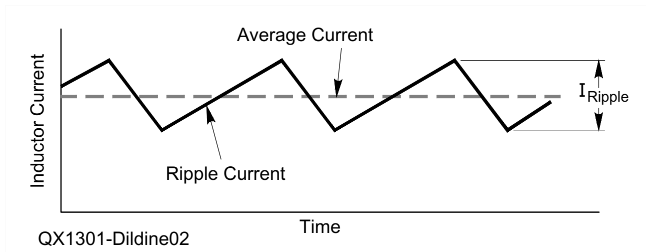

Figure 2 — Inductor current. Current increases when S1 is closed and decreases when S2 is closed.

The Math, Choosing an Inductor

Now let's look at the math that describes what's going on. The current through the inductor, I_L is made up of the average current which is equal to the load current, and the ripple current which is the change in current as the switches are opened and closed. See Figure 2.

The peak to peak ripple current is usually set to be about 30% to 40% of the load current at the start of the design and it is related to the voltage across the inductor by the familiar expression...

$$v = L\frac{di}{dt}$$

Integrating and solving for *i*, we have

$$i = \frac{1}{L}\int v\,dt$$

or simply

$$I_{Ripple} = \frac{1}{L} V \Delta t$$

When the inductor is charging, V is the voltage across the inductor, V_{in} -V_{out} and Δt is the time that S1 is closed. When the inductor is discharging, V is simply V_{out} and Δt is the time S2 is closed. (Of course this assumes there is no voltage drop across the switches, which in practice is not the case but we'll deal with that later.) It should be obvious that I_{Ripple} is the same for the two cases, when S1 is closed and when S2 is closed, so

$$I_{Ripple} = \frac{1}{L}\left(V_{in} - V_{out}\right)\Delta t_{S1} = \frac{1}{L}V_{out}\Delta t_{S2}$$

Solving this equation for the ratio of V_{out} to V_{in}

$$\frac{V_{out}}{V_{in}} = \frac{\Delta t_{S1}}{\Delta t_{S1} + \Delta t_{S2}} = S1's\ duty\ cycle$$

which is what we said in the first paragraph.

From the expression for ripple current we can choose values for the inductor and the switching frequency. Notice that for a given current and voltage difference, the inductor value is proportional to Δt. In other words, the greater the switching frequency, the lower the required inductor value. But losses in the inductor and switches increase with frequency so there's a practical limit. With modern parts this limit is around 1 MHz.

Let's take a simple example based on the circuit in figure 1. Say we have a 12 volt source and we need to supply the load with 5 volts at 0.6 amps. Let's choose a switching frequency of 300 kHz and assume a ripple current of 33% of the load current. What value inductor is needed? Taking the above equation for ripple current and solving for L we have...

$$L = \frac{(V_{in} - V_{out})\Delta t_{S1}}{I_{Ripple}}$$

S1's duty cycle (the converter duty cycle) is the ratio of the input voltage to the output voltage.

$$\frac{5Volts}{12Volts} = 0.417$$

The period of the switching cycle is

$$\frac{1}{300kHz}$$

or 3.33 microseconds so

$\Delta t_{s1} = 0.417 * 3.33$ 1.388 microseconds. The ripple current is 0.33*0.6 = 0.2 amps. So the required inductance is

$$L = \frac{(12V - 5V) * 1.388\mu s}{0.2amps} = 48.6\mu H$$

As a check, we'll use the equation for ripple current during the time when S2 is closed:

$$I_{Ripple} = \frac{1}{L} V_{out} \Delta t_{S2} = \frac{1}{48.6\mu H} * 5V * (3.33\mu s - 1.388\mu s) = 0.2amps$$

which is what we started out with.

Notice a couple of things about the inductor value. It's proportional to the time that S1 is on which implies that it's inversely proportional to the switching frequency. And it's inversely proportional to the ripple current which implies that it's inversely proportional to the load current. So as the switching frequency increases, you need less inductance and as the load current increases you need less inductance. But this also means that for a certain value of inductor there is minimum practical load current. It's sort of analogous to the critical inductance in a choke input filter for a traditional linear power supply.

Besides the inductance value, there are two other important things to consider when choosing an inductor: dc resistance of the winding and core saturation. The dc resistance must be low enough that resistive losses are not a problem and the core must be big enough that it doesn't saturate with the peak ripple current. Of course the core size will depend on the material. In Linear Technology's Application Note 35, Jim Williams gives some advice on empirically choosing an inductor from the junk box[1]. For the maximum performance, it's best to use a more analytical approach as outlined in most switching converter data sheets.

The Output Capacitor

Now what about the output capacitor? Its purpose is to filter the inductor's ripple current and make a nice clean dc voltage on the output. So it needs to store enough charge to hold the output voltage constant over the inductor's charge-discharge cycle. Another way of looking at the output capacitor is that it bypasses the inductor's ripple current to ground, so its impedance (its reactance X_c plus its equivalent series resistance, ESR and its equivalent series inductance, ESL) must be low enough that the ripple current times the impedance is less than the desired output voltage ripple:

$$V_{Ripple} = I_{Ripple}[ESR - j\frac{1}{8fC} + j4f(ESL)]$$

where f is the switching frequency. Note that the factors 8 and 4 in the above equation would normally be 2π for sinusoidal waveforms but the ripple current here is triangular[2]. When the switching frequency is in the 10s or 100s of kilohertz or higher, relatively small values of capacitors can be used, but they need to have low ESR. For example, the reactance of a 22µF capacitor at 300 kHz is about 25 mΩ. If the ESR is also about 25 mΩ, the total impedance is about 35 mΩ. Monolithic ceramic capacitors are a good choice, as they often have ESRs of 10 mΩ or less. But be careful to choose capacitors with X7R or X5R dielectrics, as the high dielectric ceramics such as Y5V or Z5U have very poor temperature and voltage coefficients and can lose a significant portion of their rated capacitance over temperature and at their rated voltage. Even the X7R and X5R capacitors have poor voltage coefficients and can lose up to 80% of their capacitance at their rated voltage. So it's a good idea to use a capacitor with a rated voltage several times higher than the supply's output voltage. This also improves the capacitor's reliability.

[1]Notes appear on page 9.

The Input Capacitor

In Figure 1 the input voltage is shown as an ideal voltage source with infinite current capacity and no resistance. All real voltage sources have a finite current capacity and some finite resistance as shown in Figure 3 so an input capacitor is used to store charge and smooth out the current drawn from the source. When S1 is closed, the input current is the inductor current that we've already seen is an increasing ramp as shown in Figure 2. The average value during the time S1 is closed is the same as the output current. When S1 is open, the input current is zero. So the input current to the supply can be approximated by a rectangular pulse of magnitude equal to the load current and duty cycle equal to the duty cycle of S1. The dc component of the input current is the average of this rectangular pulse and is simply S1's duty cycle times the load current[3]. The capacitor supplies the input current's ac component and the RMS value of the input capacitor current is $I_{RMS} = I_{LOAD}\sqrt{D(1-D)}$ where D is the converter's duty cycle (S1's duty cycle). (This expression or variations of it[4] shows up without explanation in most switching regulator data sheets and application notes. See the sidebar for the derivation.) Strange as it may seem, the input capacitor is chosen based on its ESR and current rating rather than its capacitance value. As with the output capacitor, low impedance at the switching frequency is what's important to minimize the input ripple current ripple that the source sees. Since monolithic ceramic capacitors have ESRs on the order of 10 milliohms or less, choosing a capacitance that yields a reactance of about that value or less is a good start. To further minimize input ripple current an inductor can be inserted before the input capacitor.

The Switches

Well this is all fine, but where do we

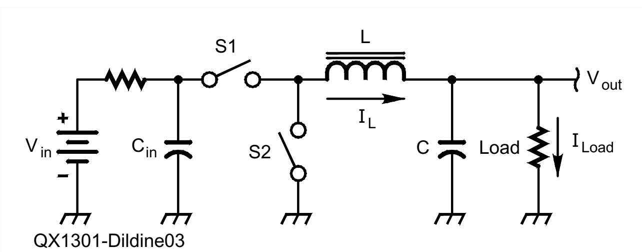

Figure 3 — Including an input capacitor.

get a couple of switches for S1 and S2 that are lossless and can be thrown at a several hundred kilohertz rate? The answer is modern power MOSFETs and Schottky diodes. While they're not completely lossless, modern power FETs come close with typical on resistances on the order of 10 mΩ or less. Replacing S1 in Figure 1 with a MOSFET and S2 with a Schottky diode we have the circuit of Figure 4.

Q1 takes the place of the switch S1 and D2 simply steers the inductor's discharge current to the load. D2 is analogous to a rectifier diode. Q1 is turned on and off at the switching frequency by a genie that lives in the magic box and controls the duty cycle while watching a voltmeter connected to *Vout*. But notice that now during the inductor discharge time the diode is in series with the load so the voltage drop across the diode represents power lost. In high current applications or low voltage applications where the diode drop is a significant portion of the output voltage, we may not be able to tolerate the power lost in the diode. If we're willing to add a little complexity and give the genie in the magic box more work to do, we can replace the diode with another MOSFET as shown in Figure 5.

Here switch S2 is replaced by Q2 which is turned on and off by our genie synchronously with Q1. It is analogous to the synchronous rectifier sometimes used in the old vibrator power supplies and so this circuit is referred to as a synchronous converter. (*Synchronous* refers to the two MOSFETs being synchronized to each other, not to some external frequency reference.) Since modern MOSFETs have very low on resistance, minimal power is lost through Q2 during the inductor discharge period.

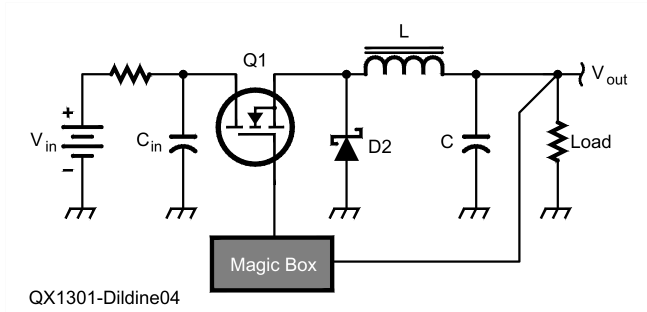

Figure 4 — A buck converter with a MOSFET and diode rectifier.

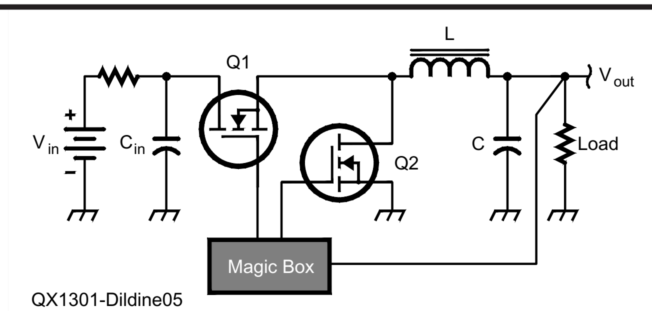

Figure 5 — Adding a MOSFET synchronous rectifier.

The Controller

That's all well and good, but where do we find a magic box with a genie inside to do our bidding? The answer to this one comes in the form of integrated switching supply controllers available from all the major IC companies. Even the simplest controllers include an oscillator to generate the switching frequency, all the necessary FET drive circuitry, and a feedback loop to regulate the output voltage by controlling the FET duty cycles. Some also include the FETs and some even include the inductor.

Real-World Components

So far we've assumed either perfect ideal components or at least they're pretty good. How do real-world components affect efficiency? As mentioned before, there will be loss in the inductor due to its dc resistance. The inductor will also dissipate power due to core losses which will increase with higher switching frequency. In a non-synchronous converter using a Schottky diode in the place of switch S2, power is lost due to the voltage drop in the diode. As mentioned above, this can be mitigated at the cost of extra complexity by replacing the diode with a MOSFET in a synchronous converter.

The power lost through the series FET, Q1 is due not only to its dc on resistance, but also to transition losses caused by pumping current into and out of its Miller capacitance. So while it's best to select a low resistance FET for Q2, you need to balance the FET's Miller capacitance against its on resistance for Q1. Most manufacturers of integrated switching controllers give a good explanation of FET losses, including the effects of Miller capacitance, in their data sheets and application notes.

Further Resources

I've only scratched the surface of buck converters, but hopefully some of the mystery has been removed and I've shown that the basic operation isn't rocket science. But as always, the devil is in the details and although it's relatively easy to get a simple buck converter working with the modern controllers, optimizing the design for maximum efficiency, minimum ripple, and all the other parameters that make a high performance circuit can be complex.

Fortunately there are a lot of resources that can help the designer. First and foremost are the data sheets of the various controllers that are available. Even carefully reading the data sheets for parts you may not consider can yield a lot of useful information. Various manufacturers offer detailed application notes describing both specific parts and generic examples of switching supply design. Particularly well written are those by Jim Williams of Linear Technology Corporation[5].

There are several simulation tools that are quite useful for switching supplies and circuit analysis in general. *LTSpice*[6] is a free general purpose SPICE simulator with particular emphasis on efficient simulation of switching supplies built around Linear Technology's controllers. Analog Devices also offers several design and simulation tools for their controllers[7] although they are more specialized. And Texas Instruments offers *TINA*[8], another free SPICE simulator.

Notes

[1]Williams, Jim, *Step-Down Switching Regulators*, Linear Technology Corporation, Application Note 35, p. 22.

[2]Analog Devices Inc., *ADP1829 Data Sheet*, p. 16. (**www.analog.com/static/imported-files/data_sheets/ADP1829.pdf**)

[3]In this regard, a buck converter can be thought of as a "dc transformer" where the turns ratio is converter's duty cycle. In the

Input Capacitor RMS Current

So where does that expression for input capacitor current come from? Let's take a look. The input capacitor current can be approximated by the trapezoidal pulse shown in Figure A1.

Here we assume the current drawn from the input source is constant and equal to I_{AV}. This is especially true if the input capacitor is preceded by a small inductance to smooth the current variations from the input source. During the time S1 is closed and the inductor is charging, the inductor current is supplied from both the capacitor and the input source. The average inductor current is equal to the load current, I_{Load} so the current drawn from the input capacitor is the difference between the load current and the current from the input supply, I_{AV}. Because current is flowing out of the capacitor, the sign is negative: $I_{CAP} = -(I_{Load} - I_{AV})$. Remember, the input current to the buck converter is simply the load current times the duty cycle, D so,

$$I_{CAP} = -\left(I_{Load} - DI_{Load}\right) = -I_{Load}\left(1 - D\right)$$

When S1 is off, the input capacitor regains the charge lost. No current is flowing into S1 so all of the current from the input source is flowing into the input capacitor: $I_{CAP} = I_{AV} = DI_{Load}$. Now current is flowing into the capacitor so the sign is positive.

The RMS value of the waveform in figure A1 can be calculated by remembering the definition of RMS: the (square) Root of the Mean of the Squares. All this means is that we take the area under each part of figure A1's waveform and square it, then add the results and divide the total by the total time covered by each part of the waveform. Finally we take the square root of the whole thing. It's easier to do it than explain it:

$$I_{CAP}RMS = \sqrt{\frac{\left[-I_{Load}(1-D)\right]^2 D + \left[DI_{Load}\right]^2 (1-D)}{D + (1-D)}}$$

The $[-I_{Load}(1 - D)]^2 D$ term represents the area under the waveform when S1 is on and the $[DI_{Load}]^2 (1 - D)$term represents the area under the waveform when S1 is off. The denominator $D + (1 - D)$, is the time of the whole cycle and is of course just 1. So simplifying the expression for RMS current,

$$I_{CAP}RMS = I_{Load}\sqrt{D(1-D)}$$

Where D is the converter's duty cycle.

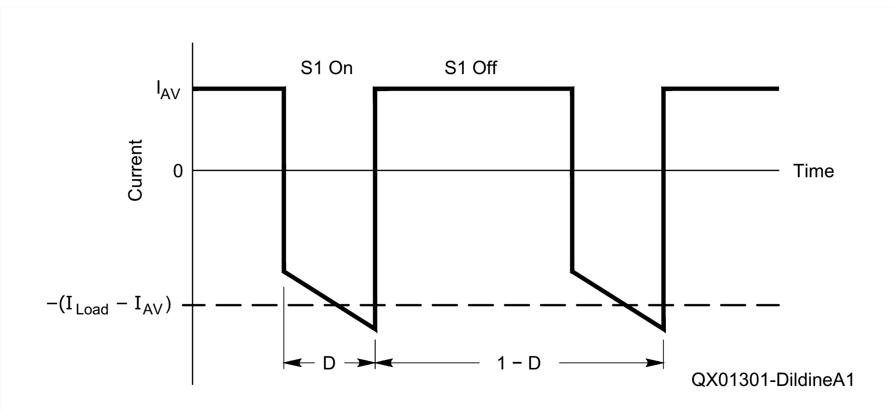

Figure A1 — Input capacitor current.

ideal case, the output voltage is the input voltage times the duty cycle and the output current is the input current divided by the duty cycle.

[4]Seemingly widely differing expressions for the input capacitor's RMS current are given in various data sheets and application notes. By remembering that the converter's duty cycle is the ratio of output voltage to input voltage, $D = V_{out}/V_{IN}$, these differences can usually be reconciled.

[5]See for example Application Notes 25 and 35 by Jim Williams as well as Application Notes 19 and 44 by Carl Nelson, all published by Linear Technology Corporation.

[6]**www.linear.com/designtools/software/#LTspice**

[7]**www.analog.com/en/power-management/products/cu_eval_pmp_tools/fca.html**

[8]**www.ti.com/tool/tina-ti**

First licensed in 1957 as WN6SFH, Bob Dildine has been primarily interested in the technical aspects of Amateur Radio. He received a BSEE degree from San Diego State College in 1967 and an MSEE from the University of California at Berkeley in 1973. He then joined Hewlett-Packard as a research and development engineer where he has done precision analog design on microwave synthesizers and network analyzers. Bob retired from Agilent Technologies in 2003 and continues to enjoy designing and building Amateur Radio projects, as well as restoring vintage electronic equipment. QEX