

# Synthesizing an Audio AGC Circuit

*Learn the steps involved with developing an AGC circuit suitable for your next receiver project.*

While experimenting with my Ultra-RX1 ultrasonic receiver, to receive CW at 40 kHz, I found the volume deafening. The receiver was designed to hear bat and insect “conversations,” which are generated at a much lower sound pressure level (SPL). The TR40 CW transmitter I used puts out a pressure wave 20 dB above that. To cure this problem, I designed an automatic gain control (AGC) circuit and incorporated that into the receiver. It then occurred to me that this simple yet elegant circuit might be useful in minimalist Amateur Radio receivers such as direct conversion QRP projects. This article presents my thinking in working through the design, and presents a stand-alone AGC circuit with a bill of materials.

The goal of adding AGC to a receiver system or audio circuit is to limit the output volume to a tolerable level when the signal becomes larger than an arbitrary reference level. A majority of the circuits you’ll find to accomplish this task place a voltage controlled attenuator in front of a fixed high gain amplifier, or modify the amplifier’s gain, each with a dc voltage derived from the amplifier output. I chose to use the variable attenuator method since I planned to implement the amplifier with a fixed gain operational amplifier (op-amp). The block diagram and desired system response are shown in Figures 1A and 1B.

## Choice of Attenuators

There are a number of choices for attenuators: MOSFETs, JFETs, LED-photocell combos, custom ICs, and more. I opted to use a MOSFET, since they are cheap and readily available. Instead of randomly searching for what works on the bench, I

measured the drain-to-source resistance of a 2N7000 N-channel MOSFET to check the range of dc feedback voltages required for the given resistance range. I used a 9 V battery, a 10 kΩ potentiometer across the gate and source and an ohmmeter across the drain and source. The results are graphed in Figure

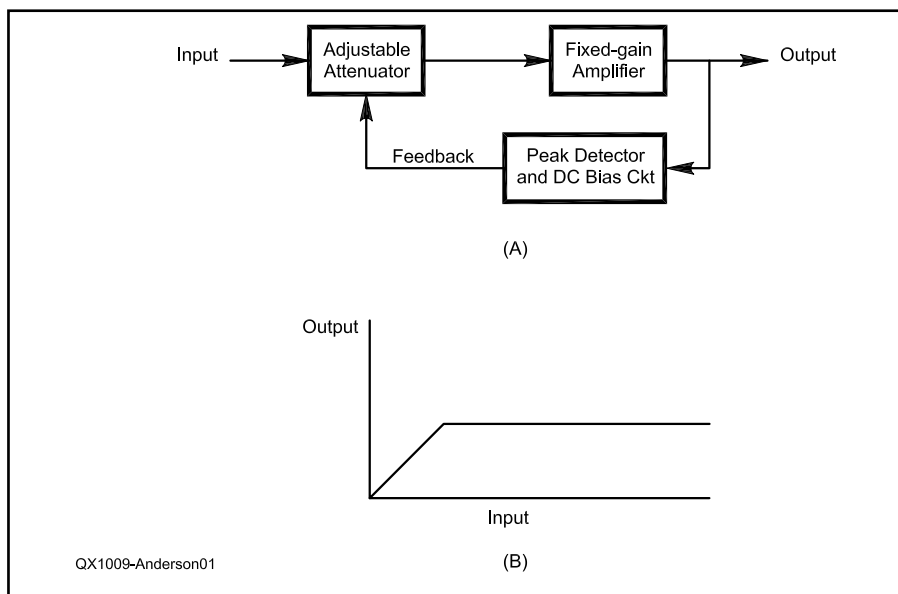


Figure 1 — Part A shows the block diagram of the AGC system and Part B graphs the system response.

**Table 1**  
Gate Voltages Required for a Given Drain-Source Resistance

*Vout/Vin, assuming preamp gain of 50*

	20	40	80	160	320	640
Vin mvpp	20	40	80	160	320	640
Vout vpp	1.2	1.2	1.2	1.2	1.2	1.2
Attenuator	0.5	0.25	0.125	0.0625	0.03125	0.015625
Rbias	4.70E+04	4.70E+04	4.70E+04	4.70E+04	4.70E+04	4.70E+04
Rp		15667	6714	3133	1516	746
Rds		23500	7833	3357	1567	758
Vgs of FET		2.24	2.35	2.39	2.40	2.40

2 and tabulated in Table 1.

Note that the resistance of the 2N7000 approaches a minimum with a high gate voltage; and achieves a nominal resistance of 23 k $\Omega$  for 2.2 V dc bias. The useful range of resistance is about 80 k $\Omega$  to about 500  $\Omega$ . *These facts dictate the gate bias voltage for the FET required from the peak detector*, as noted in Table 1. See Sidebar 1 for a derivation of the formulas used for the spreadsheet.

### Choices for a DC Control Circuit

There are a number of circuit choices for the peak detector and filter. Perhaps the most common is the op-amp derived peak detec-

tor followed by a passive RC low-pass filter. Figures 3, 4 and 5 present evolving choices from this starting point.

Figure 3A displays a popular textbook version of an op-amp based peak detector.<sup>1</sup> A positive peak detector is constructed using an op-amp with diode and resistor feedback and parallel cap and resistor to ground as the load. When the + input of U1 exceeds the - input, the op-amp output goes high, causing D1 to conduct, charge C2 and lock the - input voltage to the same level as the + input. When the + input then drops below that of the - input,

<sup>1</sup>Notes appear on page 27.

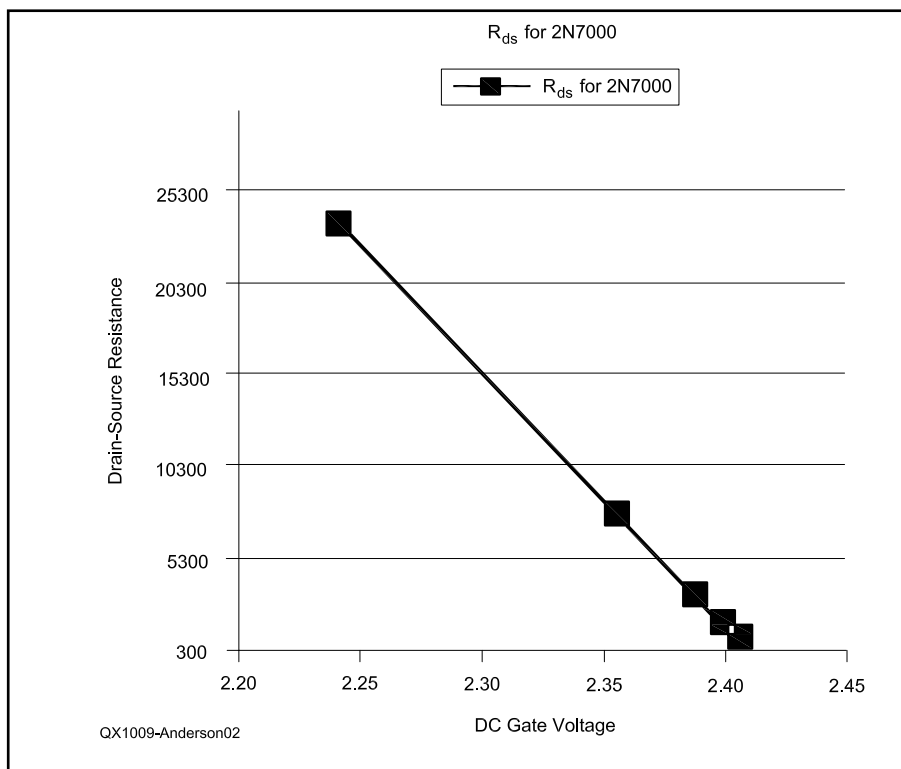


Figure 2 — A graph of the Drain-to-Source Resistance of the 2N7000 FET.

Table 2

### Bill of Material

Qty	Designation	Item	Mouser #
1	Q2	2N7000 MOSFET	511-2N7000
1	U1	4580 op-amp, 8-PIN DIP	NJM4580DD
1	Q1	PN2907 PNP TRANSISTOR	512-2N7000
2	R1, R7	47k RESISTOR	291-47K-RC
2	R2, R3	100k	291-100K-RC
1	R4	10K	291-10K-RC
1	R5	470K	291-470K-RC
1	R8	18K	291-18K-RC
5	C1-C5	10 UFD	140-HTRL50V10
1	C6	22 PF	140-500N5-220J-RC

the cathode side of the diode (labeled  $V_{Bias}$ ) retains the voltage of C2 for a bit. In effect,  $V_{Bias}$  reports the peak value of the input signal plus the bias of the (single-supply) op-amp. Figure 3B graphs a typical response.

This feedback circuit worked in *Spice* simulation and when wired on the bench to control the gain of an op-amp amplifier with a resistor and 2N7000 input attenuator.<sup>2</sup> It does, however, add a second op-amp for the detector, and the bias must be adjusted below the turn-off threshold of the FET.

This later problem can be addressed by isolating the output bias from the peak detector bias, using a comparator and a reference or adding a transistor. The transistor is cheaper and is demonstrated in Figure 4. The PNP transistor acts as a diode, as in Figure 3A, while the collector allows the output bias to float. The trick here is to tie the load through a capacitor C2 to  $V_{CC}$ . Thus when the + input of the peak detector is at a larger enough minimum peak, the transistor conducts, supplying current spikes to adjust the FET bias. Once the + input of the peak detector goes high, the transistor is off, C2 recharges and the bias to the FET gate heads to ground.

While looking at this circuit with a minimalist mentality, I surmised that without any bias at the emitter of the PNP (grounding it), an ac-coupled voltage of 1.2  $V_{pp}$  inserted at the base of the PNP transistor would maintain the same output bias. At each peak of the base signal, the transistor would conduct, thus providing a current spike to raise the voltage across the bias resistor. Hence, I could remove the op-amp peak detector and capacitor attached to the emitter, resulting in a total AGC system of one fixed-gain op-amp amplifier with simplified feedback circuitry, as displayed in Figure 5A. This circuit worked in *Spice* simulation and was verified on the bench.

### The Final Circuit

Figure 6 displays the full AGC circuit: a fixed-gain op-amp and the control circuit of Figure 5 combined. Let's walk through it. The signal source and an optional input low-pass filter are represented at the left by V1, C7, R9 and C8. The attenuator, a simple voltage divider, is constructed using resistor R1 and an N-channel MOSFET, Q2. The linear operational preamplifier starts at C1 and produces an output at pin 1 of U1 connected to C4 and a load. The load could be a pot for volume adjustment. U1, pin1, also feeds the dc control circuit via C3, wherein the circuit flows right-to-left to denote it provides "feedback" to control the variable resistance of Q2 (the FET).

U1 and the passive components around it comprise the fixed gain amplifier. It's the tra-

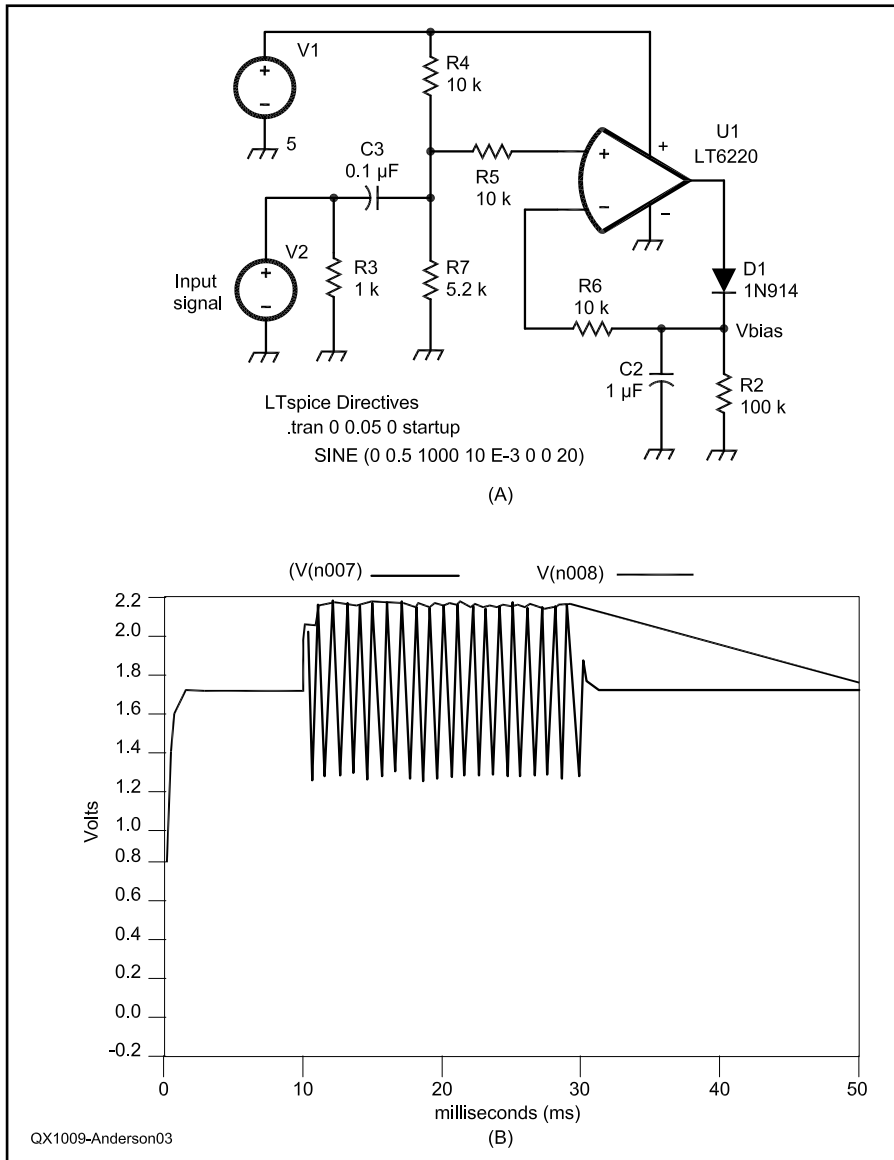


Figure 3 — Part A shows the *Spice* model circuit for a single-supply op-amp peak detector. Part B graphs the peak detector response.

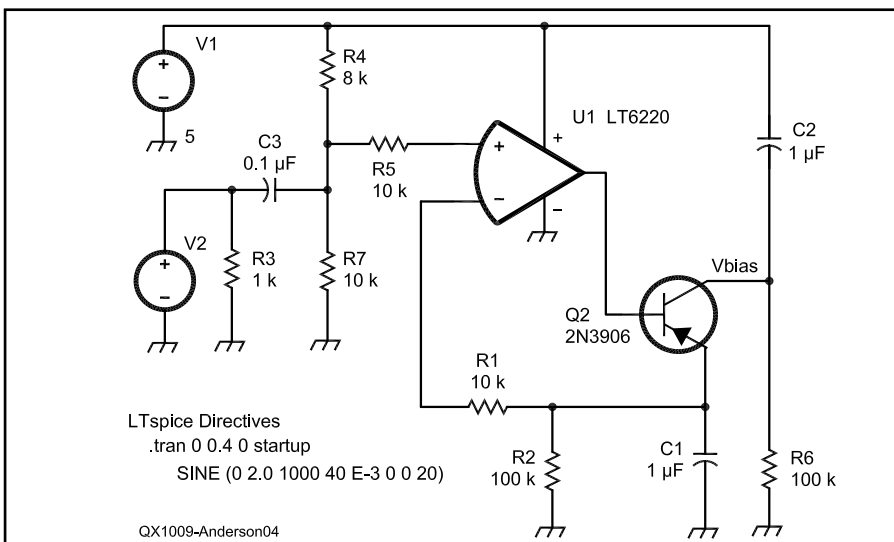


Figure 4 — This *Spice* model circuit is a peak detector with a floating output bias.

ditional single-supply configuration, biased by R2 and R3. C2 can be reduced to limit potential low frequency distortion below 300 Hz. The gain is set by feedback resistors R4 and R5. Open loop (no AGC) mid-frequency gain is the ratio of R5/R4 plus 1, or 48. C6 across R5 limits the high frequency gain a bit, but is usually optional. Most dual op-amp 8-pin ICs will work. I've tried the LMC662 and high speed NJM4580.

The control circuit shown at the bottom right consists of R6, Q1, R7, C5, and the FET. On power up — and with no signal input to or output from U1 — the voltage across C5 is charged (after a bit) to  $V_{CC}$  (+5 V dc), thus leaving the voltage on the gate of the FET at ground. With this gate voltage, the resistance of the FET from drain to source is several meg-ohms, basically turning off the AGC. During this time Q1 is off, too.

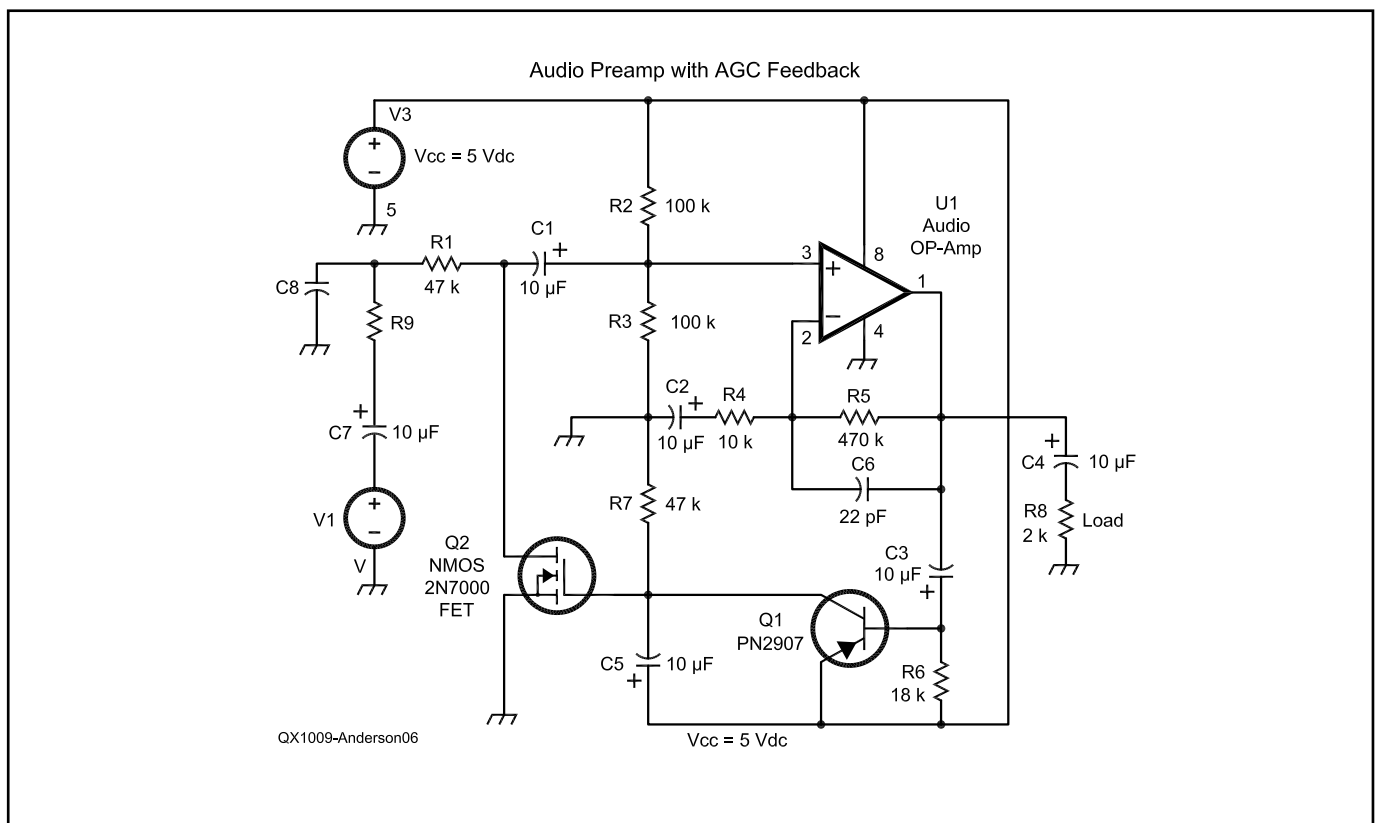
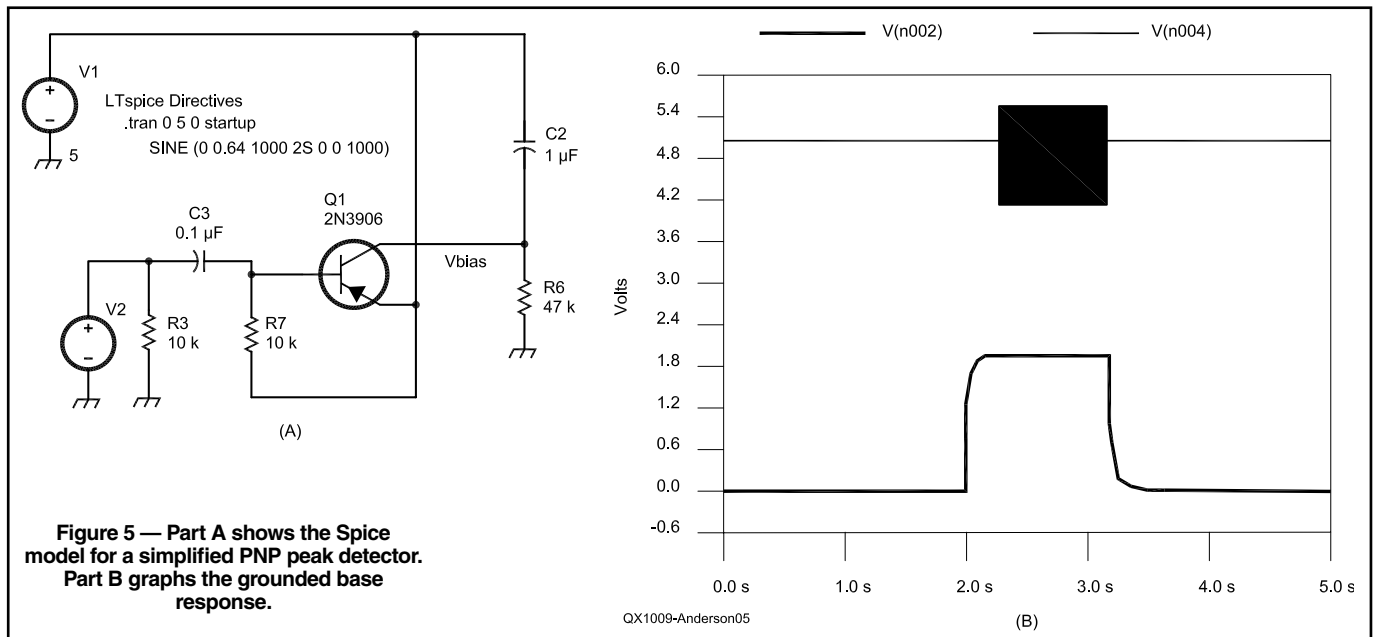
When a signal arrives and the output from U1 exceeds  $1.2 V_{PP}$ , Q1 begins to conduct when the negative peak of the ac signal at the base reaches 0.6 V, thus pulling charge away from C5 and raising the gate voltage. With a steady input signal (from V1) above  $\sim 20$  mV<sub>PP</sub>, the output of the op-amp preamp will be limited to about  $1.2 V_{PP}$ . As the output signal attempts to grow with a larger input signal, the voltage at the gate of the FET is increased, thereby offsetting the increase. The circuit holds the output signal fairly constant as the input increases over a range of better than 40 dB. A step attenuator (ref 3) fed by a signal generator with a 1 kHz to 10 kHz sine wave can be used to demonstrate the nearly constant output and increased gate voltage with an increase in input signal.<sup>3</sup>

I incorporated the circuit into the Ultra-RX2 ultrasonic receiver circuit board, shown at Figure 7. The AGC components are in the top left corner. If you try to compare the circuit schematic of Figure 6 too carefully with the board in the photo, you may find that the component designators don't match.

Since there is plenty of gain, you might consider adding this AGC circuit with pre-amp to a QRP direct conversion receiver or to a shortwave crystal radio tuner to achieve a steady volume during the reception of strong signals.

*Phil Anderson, WØXI, was first licensed as a teenager in 1953 as KNØHSB. He graduated from the University of Kansas in 1963 with a BSEE, and then earned an MSEE from Syracuse University in 1967. He added a DocEng degree from the University of Kansas in 1971. He was an engineer at IBM in Poughkeepsie, NY between 1963 and 1969. Phil founded Kantronics in 1971, and retired in 2002. He founded the Xtal Set Society in 1991, and is still playing with crystal sets!*

*In 1969 Phil took (and passed) the Novice*



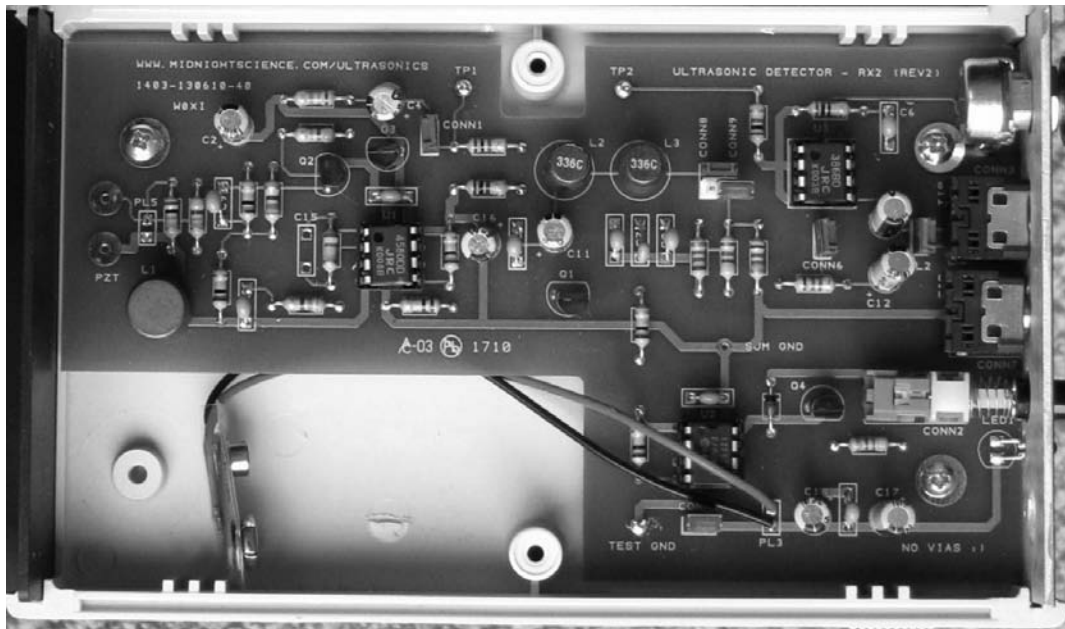


Figure 7 —The AGC circuit is incorporated into the circuit board for the Ultra-RX2 ultrasonic receiver. The AGC circuit is in the top left corner of the circuit board. Note that the component designators on the board may not match the designators on the schematic of Figure 6.

through Amateur Extra Class license exams in one sitting at the FCC Field Office in Kansas City. He is co-inventor of the GTOR communications protocol and co-designer of the Kantronics KPC-2, KPC-3, KPC-4, KPC-9612, KAM, KAM-XL and several pager controllers as well as 144, 220 and 440 MHz RF amplifiers. His current technical interests include ultrasonics, QRP, powerless devices, mm waves and radio astronomy. Phil is also a proud grandfather!

#### Notes

<sup>1</sup>An op-amp Peak Detector from any op-amp circuits text, such as Howard Berlin, *Design of OP-AMP Circuits*, H. W. Sams & Co, Inc. 1977, p 113.

<sup>2</sup>LTspice, a downloadable program from Linear Technology, used to draw and simulate circuits. See [www.linear.com/designtools/software/ltspice.jsp](http://www.linear.com/designtools/software/ltspice.jsp).

<sup>3</sup>The Step-Attenuator. Its use is described in "The Trap Coil Q Measurement Method Revisited," downloadable on this page: <https://www.midnightscience.com/article-index.html>.

<sup>4</sup>A Simple Regression calculator can be found at [www.people.hofstra.edu/Stefan\\_Waner/realWorld/regression.html](http://www.people.hofstra.edu/Stefan_Waner/realWorld/regression.html).

### Attenuator Calculations

Referring to Figure 6, the attenuator is configured as a voltage divider, with R1 as the input and the resistance of the FET and bias resistors R2 and R3 in parallel as the output. Hence, the attenuation can be written as:

$$\alpha = \frac{R_{FET} \parallel R_2 \parallel R_3}{R_1 + R_{FET} \parallel R_2 \parallel R_3} \quad [\text{Eq A1}]$$

Using a curve fitting calculator such as the one found at Note 4, a first order estimate of the FET resistance can be written as:

$$R_{FET} = mX + b = -139 \text{ k}\Omega \times V_{Bias} + 335 \text{ k}\Omega \quad [\text{Eq A2}]$$

With  $V_{Bias} = 2.24 \text{ V}$ , then  $R_{FET} = 23.64 \text{ k}\Omega$

At this operating point, with an  $R_{Bias}$  of  $50 \text{ k}\Omega$ , the attenuation,  $\alpha$ , for Figure 6 is estimated as:

$$\alpha = \frac{50 \text{ k}\Omega \parallel 23.64 \text{ k}\Omega}{47 \text{ k}\Omega + 50 \text{ k}\Omega \parallel 23.64 \text{ k}\Omega} \approx 0.25$$

