

A High-Performance Digital Transceiver Design, Part 3

Transmit functions take center stage.

By Jim Scarlett, KD7O

In Part 1, we discussed an architecture that achieves very good transceiver performance, while entering the digital domain directly from RF.¹ Part 2 showed front-end circuits for the receiver section.² In Part 3, we'll follow the transmit path from the input of the Transmit Signal Processor (TSP) to the power amplifier (PA) filter output.

Digital to Analog

The TSP circuit (Fig 1), much like its receive counterpart described in Part 2, is not terribly complex. The most difficult part of this circuit is the

package itself. Since it is a quad TSP, there is a higher pin count (128 pins), and the pins are more closely spaced (20 versus 25 mils). This makes soldering by hand something of a challenge. However, while tedious, it's not too bad. Once the corners are tacked down, it's mainly an exercise in patience.

The control interface and serial port are essentially identical to the AD6620 circuit and connect to the board on a DB25 and DB9 connector, respectively. The Microport mode is set to mode 0, so the part can be programmed in the same way as the receive signal processor (RSP). Also, even though the TSP receives serial data from the DSP, it must be the serial master. Therefore, the serial clock and frame sync for channel A are buffered, terminated and sent to the DSP serial port. The

clock rate need not be very high, since we will be using 16 bit I/Q data at sampling rates of 16 kHz and 40 kHz.

The TSP is operated at a clock rate of 70.4 MHz. This was determined by several factors. First, it is below the rated value of 75 MHz. This value allows integer interpolation of both 16 kHz and 40 kHz sampling rates. Also, the 64.96 MHz rate used in the receiver would cause the interpolation filter in the transmit DAC to cut off part of the 10 meter band. With the 70.4 MHz clock rate, the entire band is passed.

I was unable to pass the output of the TSP through a simple buffer, like I did between the ADC and the RSP in part 2. The timing was too difficult between the TSP and the DAC. I decided to latch the data and adjust the arrival time of the clock to ensure that

¹Notes appear on page 11.

Except as indicated, decimal values of capacitance are in microfarads (μF); others are in picofarads (pF); resistances are in ohms; k = 1,000.

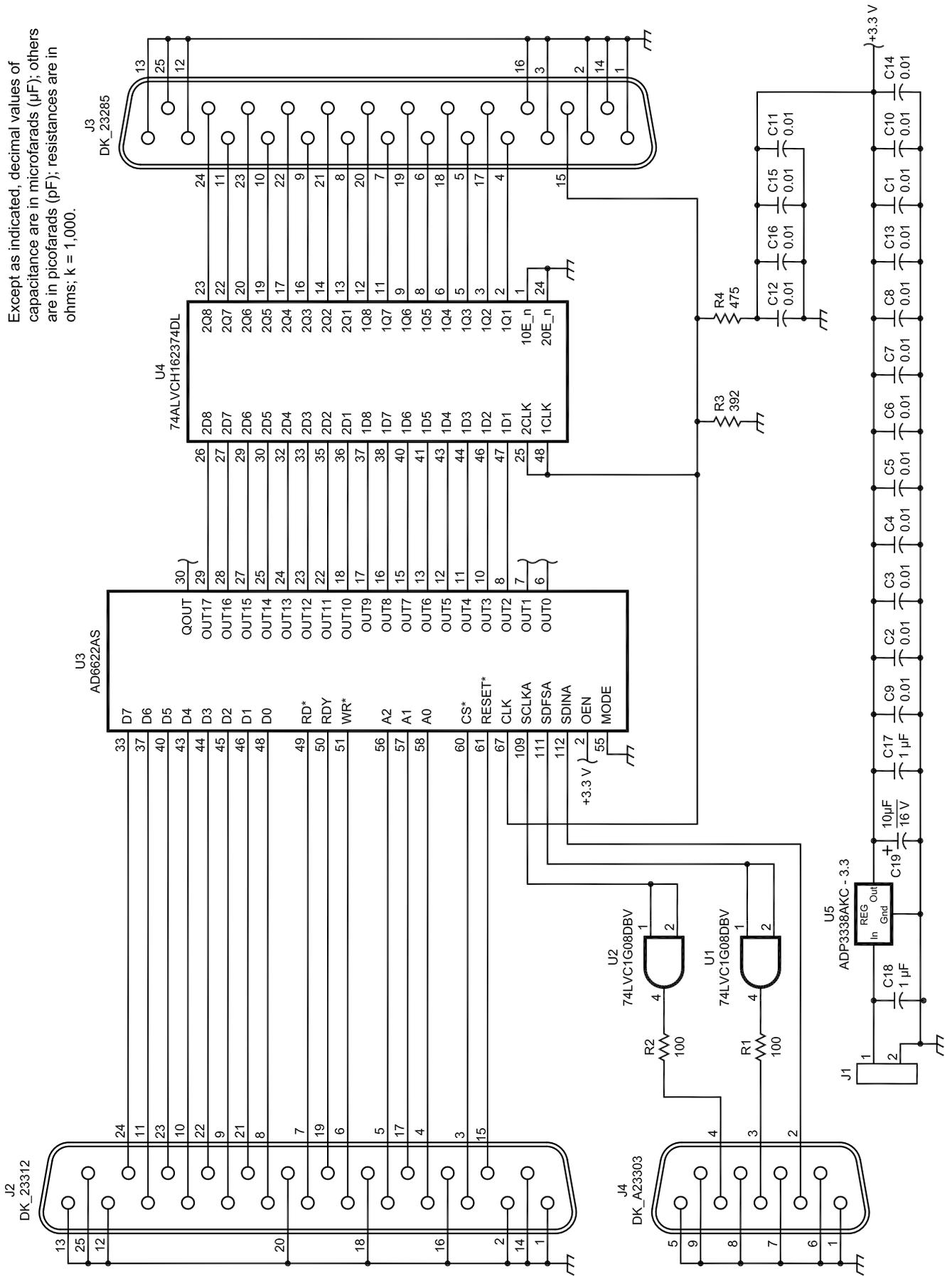


Fig 1—Transmit signal processor schematic diagram. Resistors are 0805 SMT unless otherwise noted. Capacitors are 0603 SMT unless otherwise noted. C17, C18—1 μ F 16 V X7R 1206 SMT. C19—10 μ F 16 V tantalum. J1—2 pin header. J2—DB25 right angle, PC mount (Digi-Key #A23312). J3—DB25 right angle, PC mount (Digi-Key #A23285). J4—DB9 right angle, PC mount (Digi-Key #A23303). U1, U2—Single AND gate, 74LVC1G08DBV. U3—TSP, AD6622AS. U4—16-bit latch, 74ALVCH162374DL. U5—LDO, ADP3338AKC-3.3.

the required setup and hold times were met.

I chose a 16-bit latch chip that has fast, well-defined timing parameters: the 74ALVCH162374. This part also has series termination resistors built in. The timing is straightforward between the TSP and the latch. The 70.4 MHz clock has a period of approximately 14.2 ns. The '374 is specified to latch correctly if the data is available at least 1.9 ns before the clock (setup time) and if the data remains stable for at least 0.5 ns after the clock (hold time). With this information, we know that new data from the TSP must be valid less than 12.3 ns after each clock, but that it must hold the old data at least 0.5 ns after the clock. From the specification sheet, the part will hold the old data for a minimum of 4.1 ns, and new data is valid in a maximum of 12 ns. Actual timing is likely to be somewhere between these values, but the worst case still meets our timing requirements. Timing between the latch and the DAC will be discussed shortly.

The DAC (Fig 2) is operated on a 140.8 MHz clock to take advantage of its interpolation features. A 70.4 MHz clock could have been used, but would result in more phase noise being superimposed on the transmitted signal.

Three separate 3.3 V supplies are used on the DAC board. For best performance, the datasheet recommends keeping the analog, digital and clock supplies separate, using chokes or some other means.³ I felt that the easiest (and most thorough) approach would be to use separate regulators for each.

The clock routing circuitry is quite simple. The DAC works best with differential clock input, so a 1:4 transformer is used to generate the differential signal. A dc level shift is applied to the center tap to provide the appropriate offset of $V_{cc}/2$. The center tap is also at ac ground. The resistor across

the differential signals provides balance and a proper load for the clock driver. A +1 dBm clock input will provide about 1.4 V(pk-pk) to the DAC, which will provide excellent noise performance. A +7 dBm clock input with a 1:1 transformer would do the same, but I had a 1:4 available. For best noise performance, the clock at the DAC needs to be at least 0.5 V(pk-pk).

The internal PLL is disabled by grounding the U2 PLVDD pin. A 70.4-MHz clock is now available at the PLLLOCK pin. This pin has a "fanout" of one, and therefore must be buffered. The 70.4-MHz signal is routed to the TSP and its buffer; the timing relationships involving this clock determine whether the TSP and the DAC play well together.

The period of the 70.4-MHz clock is 14.2 ns. Because of the delay involved in the generation of this clock from the 140.8 MHz input, the setup time is -1.2 ns. This means that the incoming data can arrive up to 1.2 ns after the 140.8-MHz rising edge and still be valid. This gives a total available time of 15.4 ns. The maximum delay from the clock input to 70.4 MHz output is 3.2 ns. The maximum propagation delays for the AND gate buffer and the TSP buffer are 4.5 ns and 4.6 ns. Thus, the maximum time for the arrival of the data is 12.3 ns, which provides a margin of 3.1 ns.

The minimum hold time for the DAC is 3.2 ns after the input clock rising edge. The minimum delay from the clock input to 70.4-MHz output is 2.8 ns. The minimum propagation delays for the AND gate buffer and the TSP buffer are 0.8 ns and 1.0 ns. The total minimum propagation delay is 4.6 ns, which provides a margin of 1.4 ns. Both the setup and hold times are met for the interface. Any substitutions of logic should take this timing into account.

Pins 17 and 18 (MOD0 and MOD1) set the operating mode of the device. When pin 17 is low, the interpolation filter is in the low-pass mode. This mode is set for the HF bands. By setting pin 17 high, the filter is in the high-pass mode, which is useful for adapting the transceiver to 6 m as well. Pin 18 determines whether the part is in "zero-stuffing" mode. This mode essentially performs another 2 \times upsample (with no interpolation filter), which helps to flatten out the $\sin(x)/x$ response of the DAC. The cost is that the maximum output level at lower frequencies will be 6 dB lower. Zero-stuffing is not useful for HF or 6 m, as the signal strength would decrease. I included access to this pin to allow 2-m operation if I decide in the

future to include that band.

The DAC outputs are current drivers, with the full-scale current set by a resistor on pin 40 (FSADJ). In this case, the 2-k Ω resistor sets the full-scale current at each output to just under 20 mA. The outputs feed a 1:1 transformer with a center tap. The tap is necessary to provide a dc ground, but it also allows a 6-dB voltage gain. With a 50- Ω load on the transformer output, the peak voltage at either output pin is about 250 mV. This is well within the voltage compliance range and provides some margin below the maximum output level recommended to minimize distortion.

As mentioned above, the output level from the DAC is not constant over the frequency range it will cover. This results from the $\sin(x)/x$ response of DACs. Because of the interpolation in the DAC chip, the roll-off is not as steep as it would be without interpolation. The roll-off is not too bad in the HF range, with the maximum attenuation being less than 0.7 dB at the top of the 10-m band. At 6 m (when added to the radio), the attenuation is still only about 2.2 dB.

Boosting the Power

Ignoring the $\sin(x)/x$ curve, the output of the DAC is about +4 dBm. This is fed into an emitter-follower buffer stage that runs with enough current (about 30 mA) to ensure low distortion. At the output of the buffer is a 9-dB attenuator. The 47.5- Ω resistor presents a good match for a 3-dB attenuator, since the amplifier impedance is essentially r_e , which is very low. The resistor also creates a voltage divider that provides the other 6 dB of attenuation. The attenuator performs two functions. It reduces the signal level so the next amplifier stage operates in a low-distortion mode, and it helps ensure that the band-pass filters are properly terminated.

The buffered DAC output must be filtered to prevent spurious outputs in general, and aliasing in particular. This is one of the primary benefits of interpolation in the DAC. The anti-alias filtering requirements are greatly relaxed, since one-half the sampling rate (the Nyquist bandwidth) is now 70.4 MHz instead of 35.2 MHz. The on-board digital interpolation filter takes care of most images between 35.2 MHz and 70.4 MHz, but images of 10-m signals have far less attenuation. There is some reduction; after all, the 70.4 MHz frequency was used (instead of 64.96 MHz on receive) to put 10 m in the passband of the interpolation filter.

The analog anti-alias filtering is

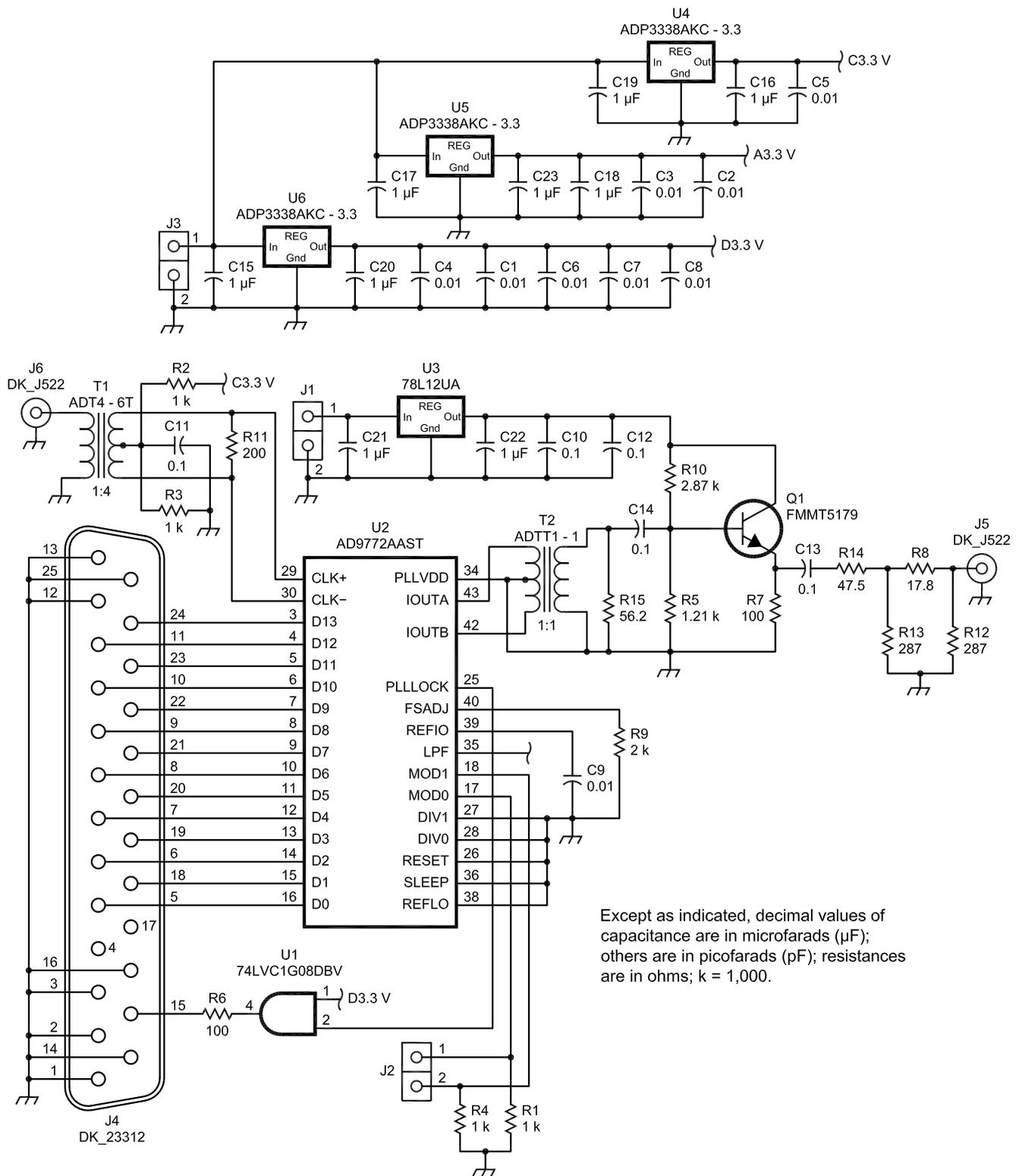


Fig 2—DAC schematic diagram. Resistors are 0805 SMT unless otherwise noted. Capacitors are 0603 SMT unless otherwise noted.

C10—0.01 μF X7R 0805 SMT.
 C11-C14—0.1 μF X7R 0805 SMT.
 C15-C23—1 μF 16 V X7R 1206 SMT.
 J1-J3—2 pin header.
 J4—DB25 right angle PC mount (Digi-Key #A23312).

J5, J6—PC mount SMB bulkhead jack (Digi-Key #J522).
 Q1—RF NPN transistor FMMT5179.
 T1—1:4 transformer, CT (Minicircuits ADT4-6T).
 U1—Single AND gate, 74LVC1G08DBV.

U2—High-speed DAC, AD9722AAST.
 U3, U4—Low power 12 V regulator, 78L12UA.
 U5, U6—LDO, ADP3338AKC-3.3.

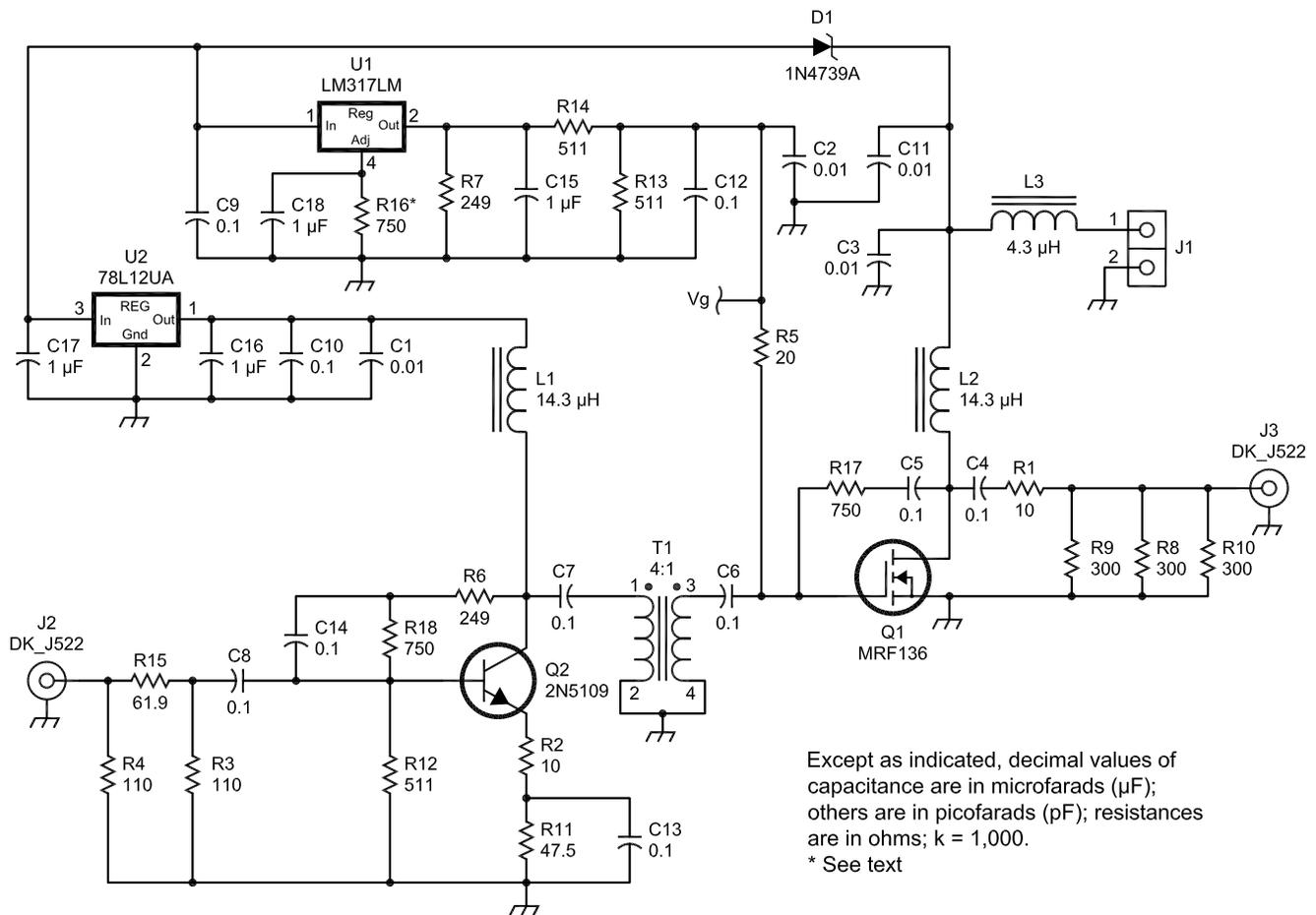


Fig 3—Driver schematic diagram. Resistors and capacitors are 0805 SMT unless otherwise noted.

C15-C18—1 μF 25 V X7R 1206 SMT.
D1—9.1 V 1 W Zener, 1N4739A.
J1—2 pin header.
J2, J3—PC mount SMB bulkhead jack (Digi-Key #J522).
L1, L2—14 t #22 AWG on a FT61-50A core.

L3—8 t #22 AWG on a FT61-50 core.
Q1—MRF136 MOSFET.
Q2—RF NPN transistor, 2N5109.
R8-R10—300 Ω 1/4 W 1206 SMT.
R11—47.5 Ω 1/4 W 1206 SMT.

R16—750 Ω test select for 300 mA drain current in Q1.
T1—BN202-43 core: secondary, 1 t (1/8-inch brass tubing), primary, 2 t #22 AWG through secondary.

done by the same filter/amplifier chain that is used on receive. On the transmit side, both amplifiers are used, to get approximately 17 dB of gain. The filtering in this chain, which was necessary to meet stringent receiver requirements, is more than enough for this application. The output is about +12 dBm.

A two-stage driver follows the filter/amplifier chain (Fig 3). One stage was not enough to reach the driver output target of 500 mW. Therefore, a two-stage design was used, with a 9 dB attenuator at the input. The attenuator keeps the amplifiers from being overdriven and provides an excellent termination for the filters. The first stage is a common-emitter BJT amplifier using emitter degeneration and shunt feedback. There is nothing unusual about this amplifier, as readers of *Solid State Design* can readily

tell.⁴ The first stage provides about 10 dB of gain.

The second stage of the driver is a common-source amplifier using an MRF136 FET. This device is capable of excellent performance well into the VHF range.⁵ The amplifier was designed with possible expansion to 6 m in mind.

The 20-Ω resistor on the gate of the FET helps ensure stability, and also makes the input easier to match across a broad range of frequencies. A 4:1 transformer completes the input network. The feedback resistor is there more to help achieve good input and output matches than for stability, which should be assured by the gate resistor. The output network consists of only a series and shunt resistor. An L-network could be added for an even better return loss, but it is not necessary for driving the PA. The driver is

mounted on the same heat sink as the PA.

Gate bias is provided via a low-power adjustable regulator. The resistance from the regulator to ground is test selected for a drain current in the MRF136 of approximately 300 mA. This is enough current to achieve excellent linearity in class-A service. The maximum output required from the driver is about 500 mW, though it is capable of much more. I think enough of the MRF136 that I'm considering replacing the receiver preamplifiers with these devices running with high currents.

Power Amplifier

The power amplifier uses a single MRF151 FET to generate a little over 60 W PEP or CW, and runs on 40 V (Fig 4). The device is capable of considerably more, but I didn't feel that I

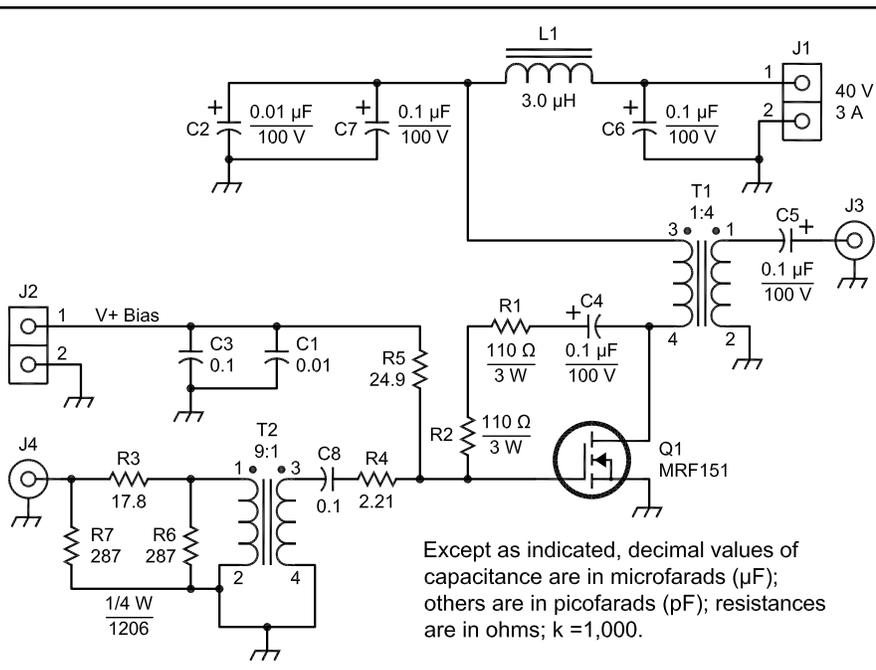


Fig 4—Power amplifier schematic diagram. Resistors and capacitors are 0805 SMT unless otherwise noted.
C2—0.01 μF 100 V.
C4-C7—0.1 μF 100 V.
J1, J2—2 pin header.
J3, J4—BNC jack.
L1—16 t #18 AWG on a T106-6 core.
Q1—MRF151 MOSFET.
R1, R2—110 Ω , 3 W metal oxide.
R3—17.8 Ω 1/4 W 1206 SMT.
R6, R7—287 Ω 1/4 W 1206 SMT.
T1—BN7051-43 core: primary, 1 t (1/4-inch brass tubing); secondary, 2 t #18 AWG through primary.
T2—BN3312-43 core: secondary, 1 t (3/16-inch brass tubing); primary, 3 t #22 AWG through secondary.

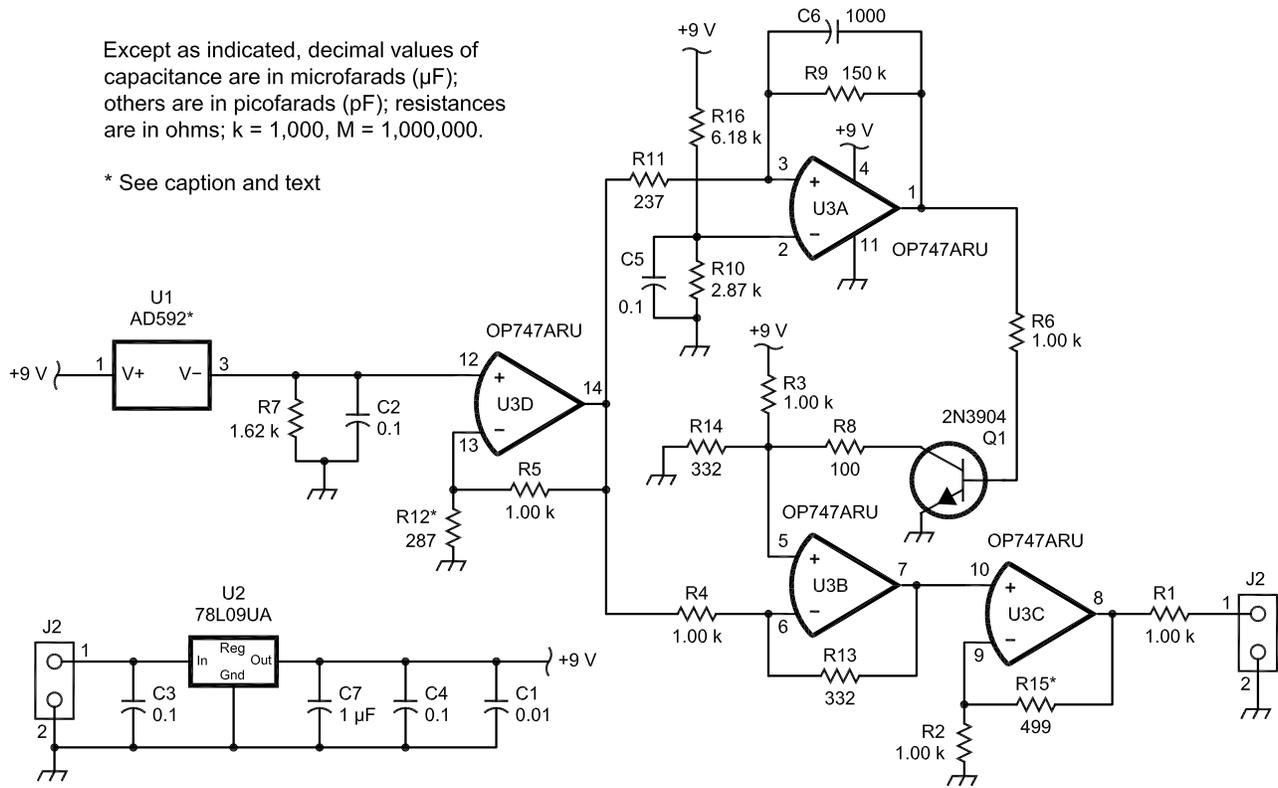


Fig 5—Power amplifier bias schematic diagram. Resistors and capacitors are 0805 SMT unless otherwise noted.

U1—AD592 temperature transducer. Mount with thermal compound on MRF 151.
U2—78L09 μA +9 V voltage regulator.
U3—Quad opamp, OP747ARU.
C7—1 μF , 25 V X7R 1206 SMT.

J1, J2—2 pin header.
Q1—NPN transistor, 2N3904.
R10—2.87 k Ω , 0805 SMT. Can be adjusted to set bias shutdown threshold.

R12—287 Ω , 0805 SMT. Test select for stable bias over temperature.
R15—499 Ω , 0805 SMT. Test select for proper bias level ($\text{IDQ} = 500 \text{ mA}$).

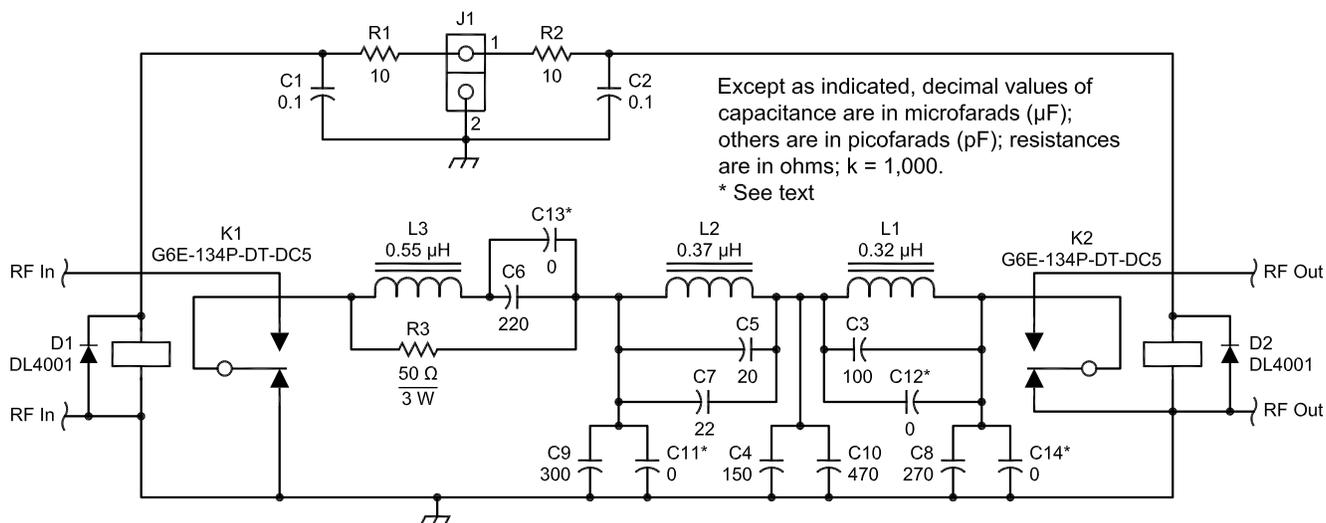


Fig 6—Transmit low-pass filter schematic diagram. Values shown are for the 20 meter filters. Component values for the other HF bands are available on the ARRLWeb (see Note 9). Resistors are 0805 SMT unless otherwise noted. Capacitors are Silver Mica unless otherwise noted.

0 pF capacitors are pads for Silver Mica capacitors.
C1, C2—0.1 µF X7R 0805 SMT.
D1, D2—DL4001.

J1—2 pin header.
K1, K2—PC mount SPDT relay (Digi-Key # G6E-134P-ST-US-DC5).
L1—0.32 µH, 13 t #18 AWG on a T106-0 core.

L2—0.37 µH, 14 t #18 AWG on a T106-0 core.
L3—0.55 µH, 17t #18 AWG on a T106-0 core.

really needed it. This power level is perfectly adequate for “barefoot” operation, and it does not tax the devices involved terribly much. It also allowed me to design the power supply mostly with parts I had on hand. I also have some plans for a 300-400 W amplifier, which would only require about 20 W of drive.

The circuit for the amplifier has a lot of similarities to that in the MRF151 datasheet.⁶ A 9:1 transformer and series resistor match the driver output with the gate of the device. I chose to use a conventional transformer with a one-turn secondary consisting of brass tubing, because of its easy construction. Like the driver circuit, a resistor is placed from gate to ground to tame the beast and broaden the input response. For this device, the recommended resistance is 25 Ω. The feedback resistance helps create decent input and output matches, and flattens the gain across the spectrum. A 1:4 output transformer provides a load line optimized for 64 W output. Again, I opted for the conventional transformer, this time with a larger core. More heat will be generated than with a transmission-line transformer (see the discussion in Note 8), but this configuration will work fine.

The bias network (Fig 5) requires some explanation. In reading about other FET amplifier projects, I noticed

a couple of different modes of thermal protection. In his 50-MHz amplifier, Dick Frey, K4XU, used thermal compensation to account for the fact that as the FET heats up, the same gate drive will induce larger standing currents (thus generating more heat).⁷ Bill Sabin, WØIYH, used thermal monitoring to shut down the devices if the temperature reached a certain threshold.⁸

I decided that I liked the idea of doing both functions, though I took a slightly different approach. Accomplishing both functions with a single temperature sensor requires a little more complexity than a single function. I used a current-output temperature sensor, the AD592, that has a more linear response than thermistors. The output of this device is 1 µA per Kelvin (at +25°C, the output is 298 µA). The TO-92 package is mounted directly on the MRF151.

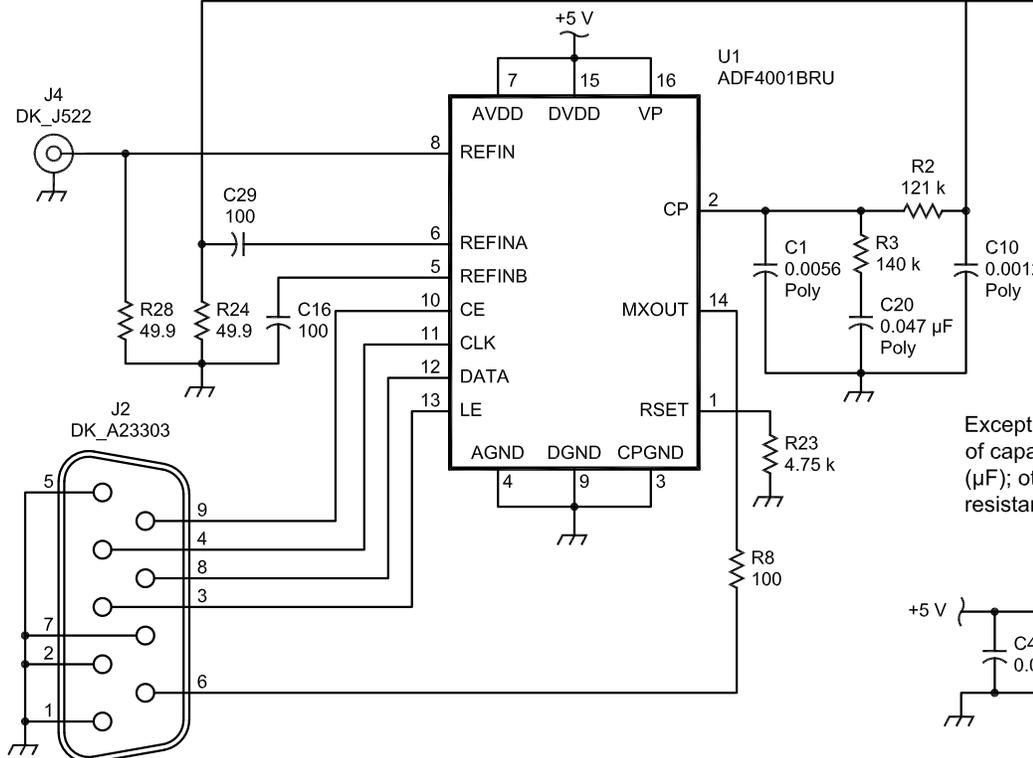
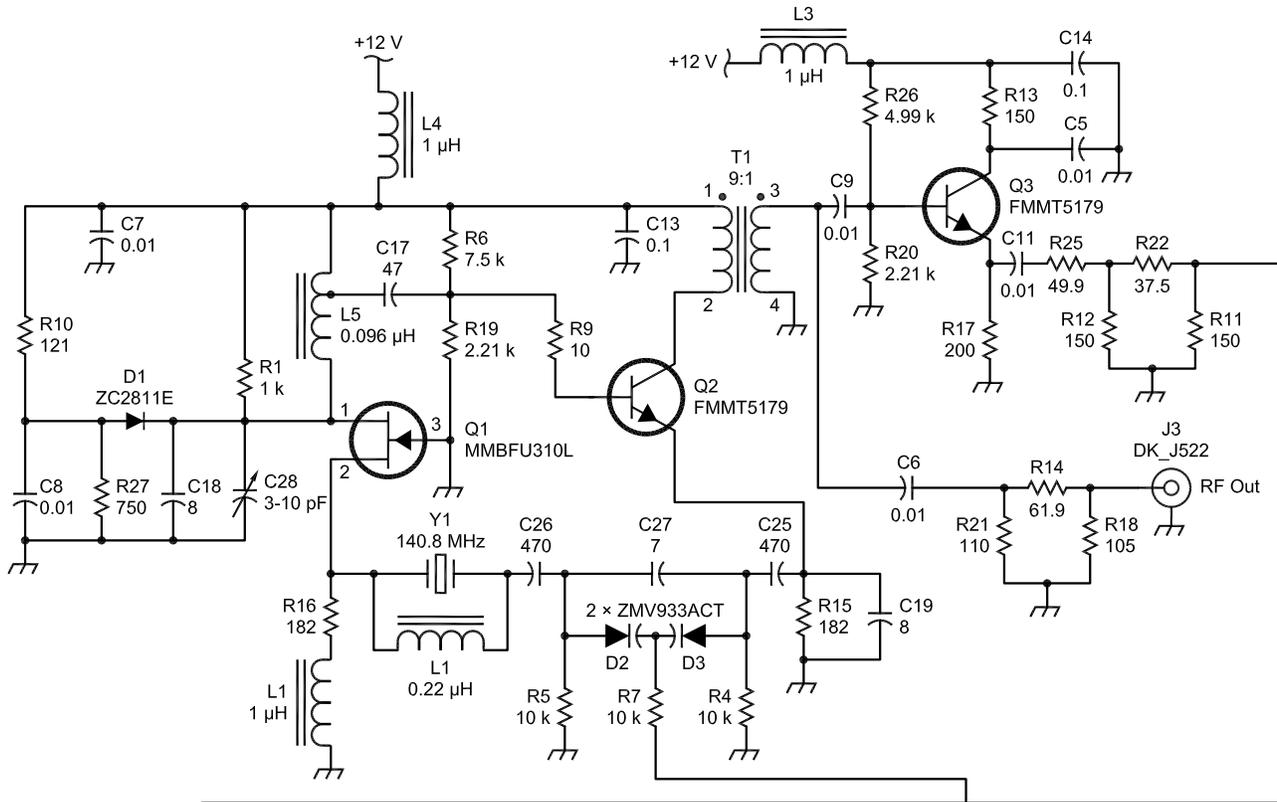
The output of the AD592 is fed to a buffer amplifier whose input uses a 1.62-kΩ resistor to convert the current signal to a voltage. The buffer has a gain of about 4.5, which sets the slope of the temperature compensation. The value of R12 can be adjusted to ensure that the bias remains constant over temperature. The buffer feeds two other amplifiers. One is a summing amplifier that combines the bias voltage with the compensation voltage. The other is used as a comparator to

clamp the summing amplifier output to about 0 V when the MRF151 temperature gets too high. The hysteresis in the comparator circuit creates a window of about 1.9°C, meaning that the temperature must drop that amount before bias is restored. The feedback capacitor changes the hysteresis for high-frequency signals, so that false triggering from this source does not occur.

The summing amplifier feeds a fourth amplifier that sets the final output. The value of R15 sets the bias point. This can be set while observing the two-tone output on a spectrum analyzer; or if one is not available, to set the I_{DQ} to about 500 mA. This last amplifier is not absolutely necessary, but I wanted to make it as simple as possible to adjust the bias. If instead the bias were to be adjusted using R13 in the summing amplifier, the value of R14 must be adjusted also. Otherwise, the compensation slope would be affected by the gain change. Besides, I still had a fourth amplifier available in the package. The calculations used for the bias network are in a spreadsheet (“PA_bias_compensation.xls”) that can be downloaded from the ARRLWeb.⁹

Low-Pass Filters

The output low-pass filters (Fig 6) are of the Cauer type. They have been optimized for suppression of the sec-



Except as indicated, decimal values of capacitance are in microfarads (μF); others are in picofarads (pF); resistances are in ohms; k = 1,000.

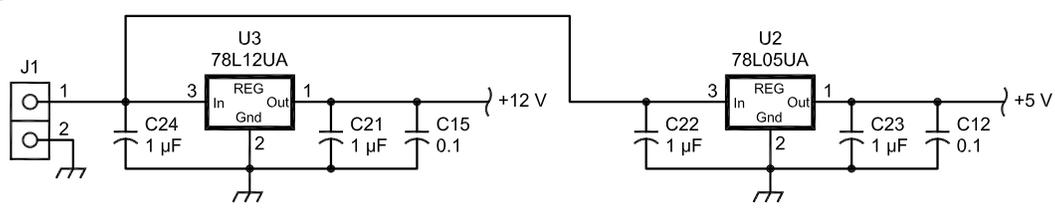
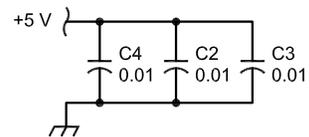


Fig 7—Transmit PLL schematic diagram. Resistors and capacitors are 0805 SMT unless otherwise noted.

C1—0.0056 μ F polyester (Digi-Key #P3562).
C2-4—0.01 μ F 0603 SMT.
C10—0.0012 μ F polyester (Digi-Key #P3122).
C20—0.047 μ F polyester (Digi-Key #P3473).
C21, C24—1 μ F 25 V X7R 1206 SMT.
C22, C23—1 μ F 16 V X7R 1206 SMT.
C28—3-10 pF trimmer, SMT (Digi-Key #SG2002).
D1—Schottky diode, ZC2811E.
D2, D3—Tuning diode (Digi-Key #ZMV933ACT).
J1—2 pin header.
J2—DB9 right-angle PC mount (Digi-Key #A23303).
J3, J4—PC mount SMB bulkhead jack (Digi-Key #J522).
L1—0.22 μ H.
L2-L4—1.0 μ H.
L5—8 t #28 AWG on a T37-12 core; tap 2 t from “cold” end.
T1—primary 6 t #28 AWG on a BN2402-61 core; secondary 2 t #28 AWG.
U1—PLL, ADF4001BRU.
U2—regulator, SOT89, 78L05UA.
U3—regulator, SOT89, 78L12UA.
Y1—140.8 MHz, seventh overtone (International Crystal).

ond and third harmonics, as described by Tonne.¹⁰ Also, they incorporate a diplexer as Stephensen demonstrated to provide a good match for the harmonics. This reduces reflections of the harmonics and improves the linearity of the amplifier output.¹¹

The iron-powder cores used in the filters were chosen to ensure that overheating would not be a problem at this power level. The objective was to keep the flux density for each inductor significantly below the maximum recommendations outlined in the Amidon data manual.¹² Accomplishing this involves larger cores and more turns, which usually don't go hand in hand. This is why, for instance, the 20-m filter inductors use the “0” material. The capacitors are the silver-mica types, with a rating of 500 V. They can easily handle the signal levels expected in the filters.

Transmit Clock

The design of the transmit clock is nearly identical to the low-noise clock used for receiving (Fig 1). Several component values have been changed to reflect the much higher frequency of operation. Also, remembering that we only need +1 dBm for the DAC clock, the output has additional attenuation.

The PLL reference frequency is 64 kHz. This is necessary because the reference oscillator frequency was selected to minimize noise in the receive PLL. Still, the final result works out pretty well. The loop bandwidth is only about 65 Hz, because the PLL noise is much higher with the large divide ratio ($N = 2200$). Inside the loop, the PLL noise dominates (the reference noise is much lower).

Outside the loop, the VCXO noise dominates. The predicted phase noise of the VCXO is quite good; though as Leeson predicts, it is not as good as the 64.96-MHz receive oscillator. However, the final noise performance on the transmit side is not considerably different than for receive. This is because of the effect that phase noise (or jitter) has on ADCs and DACs. As shown in the “Phase Noise and ADC Performance” sidebar in Part 2 (see Note 2), the effect is smaller for lower signal frequencies. So, the phase noise of the transmit clock, when applied to a 10-m signal, is reduced by about 14 dB. The noise sidebands actually applied to the desired signal in both transmit and receive are therefore quite similar.

Summary

Modern signal-processing devices can give us as much simplification in our transmitter architecture as on receive architecture. In this design, we have barely scratched the surface of what can be done with all of the flexibility built into the TSP chip. The performance of the DAC gives us a very low-noise, low-distortion output capability. DAC features, such as interpolation, give us much more flexibility in the analog design.

New devices, either released or

about to be released, are improving on even this excellent performance. They provide even more flexibility than that found in the AD9772A. For that reason, this design was done in a modular fashion, just as was the receiver. For instance, a new 16-bit DAC design can be directly interfaced to the TSP output connector to upgrade performance. As such, we can constantly improve the performance of this radio as new technology allows. Additionally, we can add new modes simply by upgrading the software or changing the configuration of the TSP.

We have now looked at the main signal-processing blocks for both receive and transmit. Next time, we will look at some of the circuits that bring it all together, including audio and control blocks. The DSP will be linked into the system as well.

I would like to thank all the gentlemen whose work is referenced in this article. Their excellent work made mine much easier.

Notes

- ¹J. Scarlett, KD7O, “A High-Performance Digital Transceiver Design, Part 1”, *QEX*, Jul/Aug 2002, pp 35-44.
- ²J. Scarlett, KD7O, “A High-Performance Digital Transceiver Design, Part 2”, *QEX*, Mar/Apr 2003, pp 3-12.
- ³Analog Devices, AD9772A datasheet, Rev A, 3/02.
- ⁴D. DeMaw, W1FB, and W Hayward, W7ZOI, *Solid State Design for the Radio Amateur*, (Newington, Connecticut: ARRL, 1977), pp 188-192.
- ⁵M/A-Com, MRF136 datasheet, Rev 7.
- ⁶M/A-Com, MRF151 datasheet, Rev 9.
- ⁷R. Frey, K4XU, “A 300-W MOSFET Linear Amplifier for 50 MHz”, *QEX*, May/June 1999, pp 50-54.
- ⁸W. Sabin, W0IYH, “A 100-W MOSFET HF Amplifier”, *QEX*, Nov/Dec 1999, pp 31-40.
- ⁹You can download this package from the ARRLWeb at www.arrl.org/qexfiles/. Look for 1103SCARLETT.ZIP.
- ¹⁰J. Tonne, WB6BLD, “Harmonic Filters, Improved”, *QEX*, Sep/Oct 1998, pp 50-53.
- ¹¹J. Stephensen, KD6OZH, “The ATR-2000: A Homemade, High-Performance HF Transceiver, Part 3”, *QEX*, Mar/Apr 2001, pp. 3-8.
- ¹²Amidon Associates Data Manual, Jan 2000, pp 1.35-1.41. □□