

A 100-W Class-D Power Amplifier for LF and MF

Get high efficiency from a complementary pair of inexpensive MOSFETs.

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Introduction

This paper describes a simple, high-efficiency transmitter for LF and MF experimental operation. The power amplifier (PA) is a class-D design using a complementary pair of MOSFETs.¹ It operates from 165 V and delivers 100 W with an efficiency of 89%. The PA is configured for operation at 500 kHz, but can be adapted to any frequency from 100 kHz to 3 MHz by changing the output filter. The driver is a single gate-driver IC, and a one-transistor circuit keys the drive for CW opera-

¹Notes appear on page 13.

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tion. The finished project is shown in Figure 1.

Note: This is a project for experienced experimenters. The 165-V dc-supply voltage can be lethal. Treat this circuit with the same respect you would give a vacuum-tube amplifier.

Driver

The driver (Figure 2) operates from +12 V and requires about 50 mA. The signal input can be a sine wave of 3 V (peak) or more (20 dBm), TTL, or a square wave of about 1 V peak or more. Resistor R101 provides a load for the signal source. It should be removed for TTL or if necessary to get a sufficient output from the signal source. An insufficient input signal can lead to chaotic oscillations at high power due to transients from the final entering the input to the driver.

U101 is a standard 4-A gate driver that converts the input signal into square-wave drive for the final. It is biased near the threshold by adjustment of R103; hence, any input signal pushes the output of U101 into either a high or low state. To adjust the threshold, remove the signal input and look at the drive output with a scope or voltmeter. Adjust R103 to increase the bias voltage until a change is observed in the drive output, then back off R101 slightly so the output of U101 rests in the low state. The resultant bias voltage is about 1.5 V. (Alternately, R101 can be adjusted so that U101 rests in the high state.)

Keying for CW operation is accomplished by turning the drive on and off. This is done by Q101 and the related components. An open circuit or greater than +9 V at the key input

J102 results in no drive, while a short circuit or 0 V turns the drive on. This allows operation from either key or a programmable waveform generator with a range of 0 to 10 V. Capacitor C110 and resistors R105 and R106 control the shape of the waveform to avoid key clicks. The value of 10 μ F produces a rise/fall time of about 10 ms.

Final Amplifier

The final amplifier (Figure 3) consists of a complementary pair of 200-V power MOSFETs Q201 and Q202. The MOSFETs are biased near the threshold of conduction by R205 and R206 so that any RF drive pushes one into an on state and the other into an off state.

Gate biases are supplied by two Zener-regulated supplies. The bias for *n*-channel MOSFET Q202 is derived directly from the +12 V supply. The source of *p*-channel MOSFET Q201 is connected to the main supply V_{DD} , which may be variable. Consequently, the bias supply for Q201 floats against V_{DD} . This is accomplished by coupling the square-wave drive signal through C205 to the floating supply consisting of D203, D204 and C206, which provides a voltage of approximately $V_{DD} - 12$ V to operate the bias circuit.

Turning both Q201 and Q202 on simultaneously produces a short circuit. Therefore, it is important to set the biases via the following procedure. Begin by disconnecting C210 and C211 and setting V_{DD} to 0. Connect the +12-V supply, then adjust R205 to produce 0 V. Apply drive, verify that the floating bias supply is working, and set R206 to produce $V_{DD} - 0$ V. Increase V_{DD} and make sure no drain current flows, then return to zero. Temporarily connect a resistor of approximately 100 Ω from the two drains to ground. Set V_{DD} to about 25 V. Slowly adjust R206 until approximately 5 mA is flowing in Q201. The resultant bias voltage is about $V_{DD} - 2.7$ V for the VP1220N5, but may be different for other MOSFETs. Turn off V_{DD} , remove the 100- Ω resistor from the drains, and connect a voltmeter in its place. Return V_{DD} to 25 V and slowly adjust R205 until the drain voltage is about 12.5 V, which implies equal quiescent currents in the two MOSFETs. The resultant bias voltage is about 3.5 V for the IRF610. The drain voltage will drift and vary with temperature, but the MOSFETs will remain sufficiently close to their thresholds of conduction for proper operation when drive is applied. Finally, reconnect C210 and C211.

The output network provides a 50- Ω load to the drains, high imped-

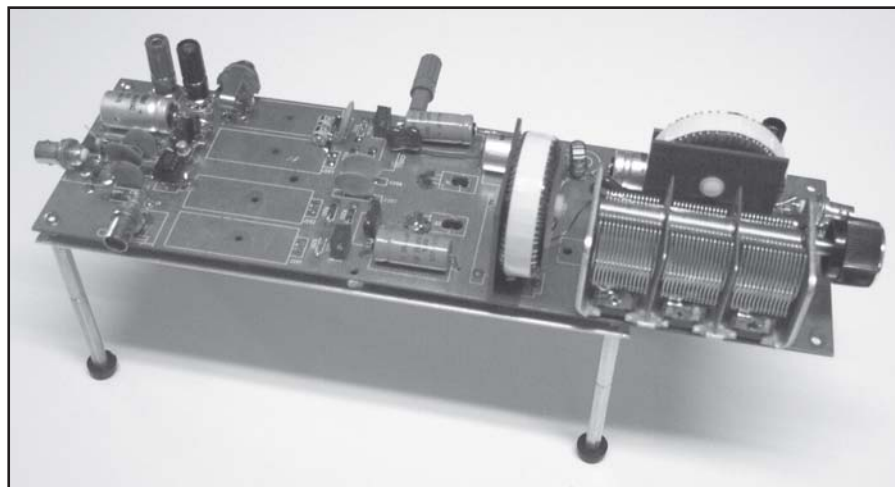


Figure 1 — The LF/MF complementary class-D transmitter.

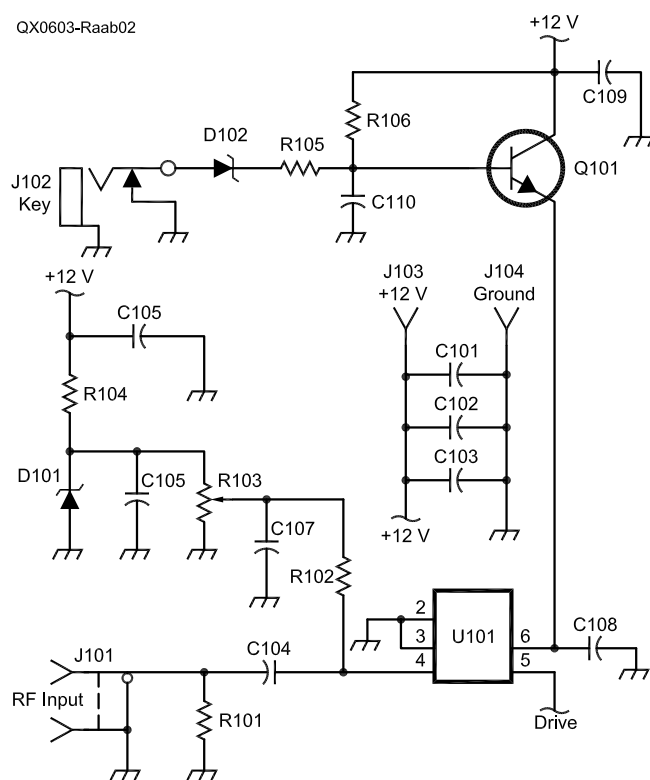


Figure 2 — Circuit of driver.

C101 — 20- μ F, 250-V electrolytic.

C102 — 3300-pF mica.

C103 — 0.1- μ F, 50-WV chip,

ATC 200B104NP50X.

C104 — 0.1- μ F disk.

C105-C109 — 1- μ F, 50-WV X7R chip,

Kemet 1210C105K5RATCU.

C110 — 4.7- μ F, 25-V electrolytic.

D101 — 1N751A, 5.1-V, 0.25-W Zener.

D102 — 1N746A, 3.3-V, 0.25-W Zener.

J101 — BNC jack.

J102 — Key jack, shorting.

J103 — European-style binding post,

red, E.F. Johnson 111-0102-001. Mount vertically.

J104 — European-style binding post,

black, E.F. Johnson 111-0103-001.

Mount vertically.

R101 — 51- Ω RC07 (omit for TTL input).

R102 — 4.7-k Ω RC07.

R103 — 5-k Ω trimpot, Bournes

3006P-1-502.

R104 — 620- Ω RC07.

R105, R106 — 2.2-k Ω RC07.

Q101 — PNP BJT, 2N2907.

U101 — 4-A gate driver, TI UCC32325P or

equivalent.

ances to the harmonics, adequate suppression of the harmonics in the output, and single-knob tuning to the frequency of operation. The T configuration may be regarded as two back-to-back L networks that match upward to about 150 Ω at the center. Inductor L201 has a Q of 3, which is sufficient to ensure that third-harmonic current circulating in the drains is no more than 10% of the fundamental-frequency current.

Adjustment is quite simple, since maximum RF output, maximum dc input, and maximum efficiency occur so close to each other that the settings are indistinguishable. Begin with V_{DD} set to 25 to 50 V. Adjust C214 for either the maximum dc power or maximum RF output. Make a quick check on the RF output (Figure 4) and the

efficiency to ensure the PA is operating correctly. Then increase V_{DD} to 100 V and tweak C214 slightly to allow for any variation of drain capacitance with voltage. Then increase V_{DD} to its full value of about 165 V without readjustment. The dc-input current should be about 0.72 A.

Performance

The waveforms are shown in Figure 4 for operation at 500 kHz from $V_{DD} = 100$ V. In this case, the input v_i is a TTL signal. The drive signal v_{DR} produced by U101 is a square wave that ranges from 0 to 12 V. The drain voltage v_D produced by the two MOSFETs is a clean square wave. The complementary configuration eliminates most of the transients associated with charging

drain capacitance through the inductance of a transformer.^{2,3} The small droops are the result of drain current flowing through the on-state resistances of the MOSFETs. The output v_O is a pure sine wave.

The output and efficiency characteristics for operation at 500 kHz are shown in Figure 5. Output voltage V_{om} varies linearly with supply voltage V_{DD} . The transfer curve fits a straight line with an rms error of only 0.2%, indicating excellent amplitude-modulation linearity (IMDs less than -50 dBc). The efficiency is about 89% over most of the output range. It drops slightly at high levels because of increased MOSFET resistance and slightly at low levels because of increased drain capacitance.

The PA can be used at frequen-

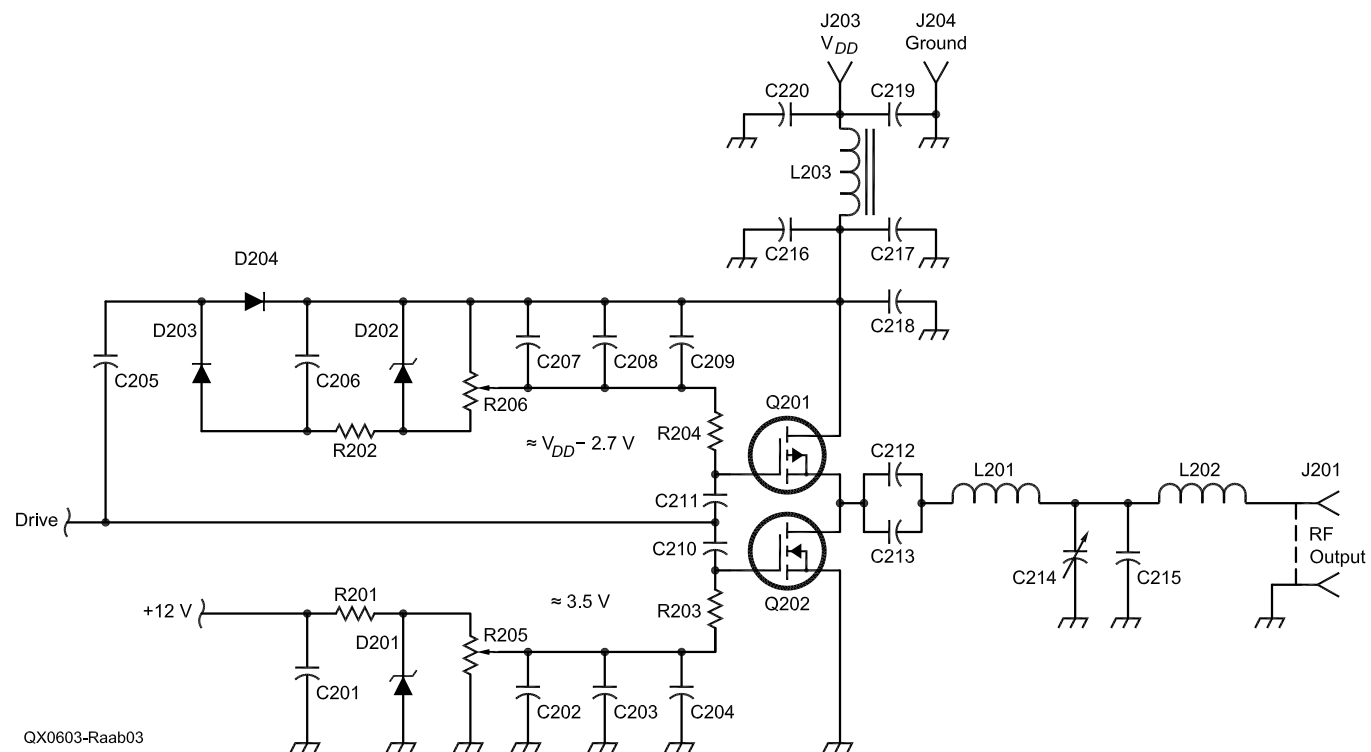


Figure 3 — Circuit of final amplifier.

C201 — 1- μ F, 50-WV X7R chip, Kemet 1210C105K5RATCU.
 C202, C207, C211 — 0.1- μ F, 50-WV chip, ATC 200B104NP50X.
 C203, C208, C215, C217, C219 — 3300-pF mica.
 C204, C209 — 5- μ F 25-V electrolytic.
 C205, C210, C211 — 0.022- μ F disk.
 C206 — 10- μ F 25-V electrolytic.
 C212, C213, C218 — 0.1- μ F, 200-WV chip capacitor (American Technical Ceramics 900C104NP200).
 C214 — Three-gang breadslicer, 15-525 pF per section, 70% closed at 500 kHz.
 C216, C220 — 20- μ F, 250-V electrolytic.

D201, D202 — 7.5-V 0.25-W Zener, 1N755A.
 D203, D204 — MUR120 60-V 1-A ultra-fast switching diode.
 J201 — BNC jack.
 J202 — European-style binding post, green, E.F. Johnson 111-0104-001.
 J203 — European-style binding post, red, E.F. Johnson 111-0102-001. Mount vertically.
 J204 — European-style binding post, black, E.F. Johnson 111-0103-001. Mount vertically.
 L201, L202 — 47.7 μ H. 61 turns #24 AWG enameled wire on Micrometals T200-2 toroid.

L203 — 30 turns #24 AWG on Ferroxcube 768XT188 3E2A toroid.
 Q201 — Supertex VP1220N5 200-V, 2-A P-channel MOSFET.
 Q202 — IRF610 200-V, 2-A, N-channel MOSFET.
 R201, R202 — 1-k Ω RC07.
 R203, R204 — 10-k Ω RC07.
 R205, R206 — 10-k Ω trimpot, top-adjustable, Bournes 3299X-1-103.
 Heat sink — Extruded aluminum, 3.75-in wide, Aavid 60675.
 Insulating pads for Q201, Q202 — Thermalloy 43-77-2.

cies from 100 kHz to 3 MHz. Its performance is shown in Figure 6 as a function of frequency. These tests are based upon $V_{DD} = 165$ V and simple series-tuned output circuits instead of the T network shown in Figure 2. The power drops from about 100 W at 500 kHz to 92 W at 3.5 MHz, and efficiency drops from about 90% to 83%.

Adaptation to Different Voltages and Powers

The basic design presented here can be adapted to other MOSFETs, supply voltages and output powers. The output power of a complementary class-D PA is:

$$P_o = 2 V_{\text{eff}}^2 / (\pi^2 R_{PA}) \quad (\text{Eq 1})$$

where R_{PA} is the drain-load resistance. The effective supply voltage is:

$$V_{\text{eff}} = V_{DD} R_{PA} / (R_{PA} + R_{on}) \quad (\text{Eq 2})$$

where R_{on} is the on-state resistance of the MOSFETs. These equations allow determination of the drain-load resistance R_{PA} for a desired output power P_o and supply voltage, or vice versa.

The T network can be regarded as two back-to-back L networks (Figure 7) that match upward to an intermediate resistance R_m , which must be larger than either the input or output resistance. The capacitor in the T network is the sum of the capacitances in the two Ls. The equations for design of the L networks (from the reference cited in Note 1, Table 3-3.1) are

$$X_L / R = -X_C / R_m = Q \quad (\text{Eq 3})$$

and

$$Q^2 + 1 = R_m / R \quad (\text{Eq 4})$$

Above, R is R_{PA} or R_o as appropriate for the input or output L. The design process can begin either by

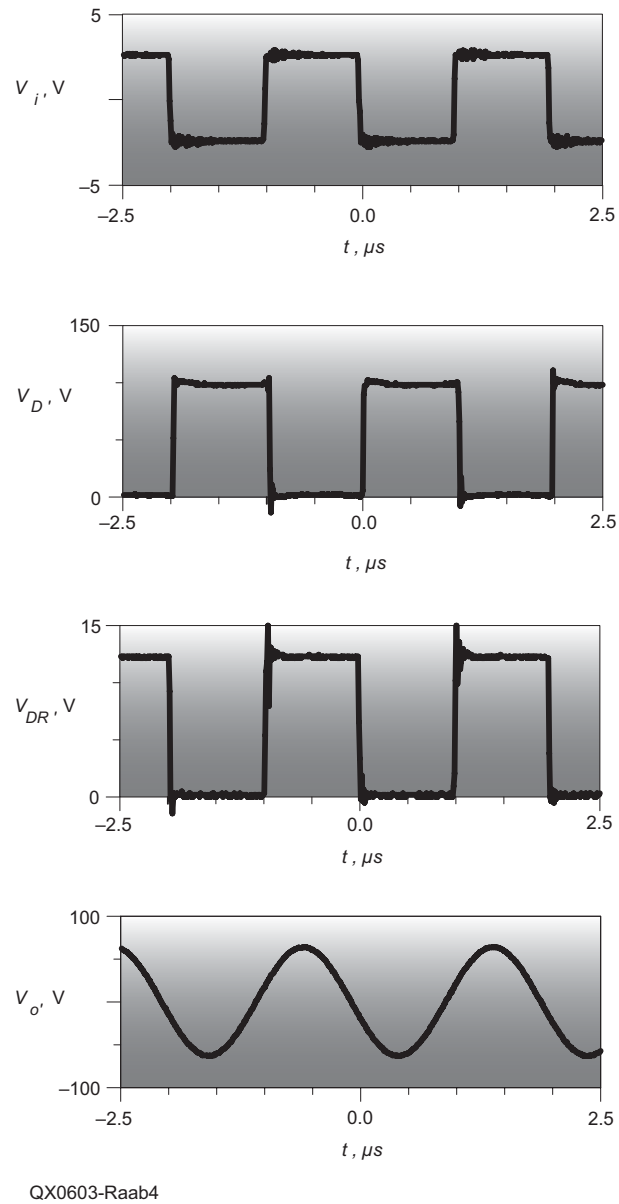


Figure 4 — Waveforms at 500 kHz.

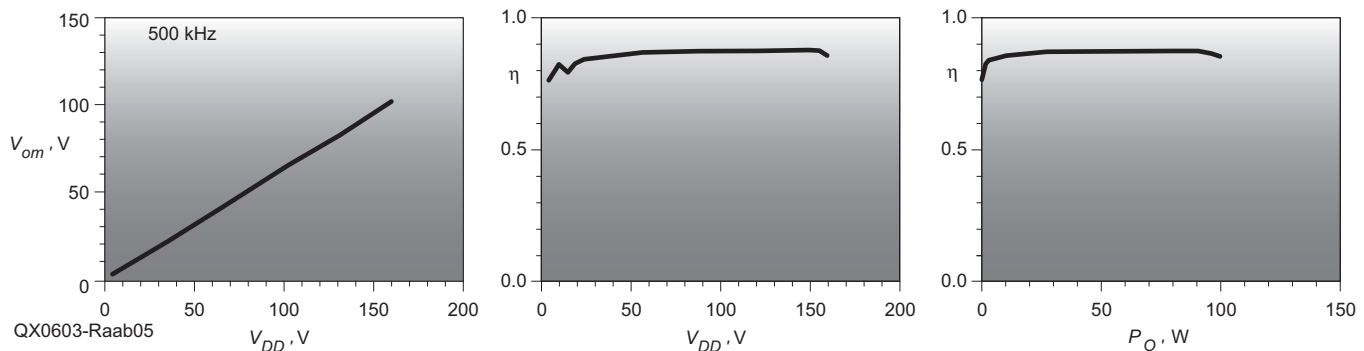


Figure 5 — Power and efficiency at 500 kHz.

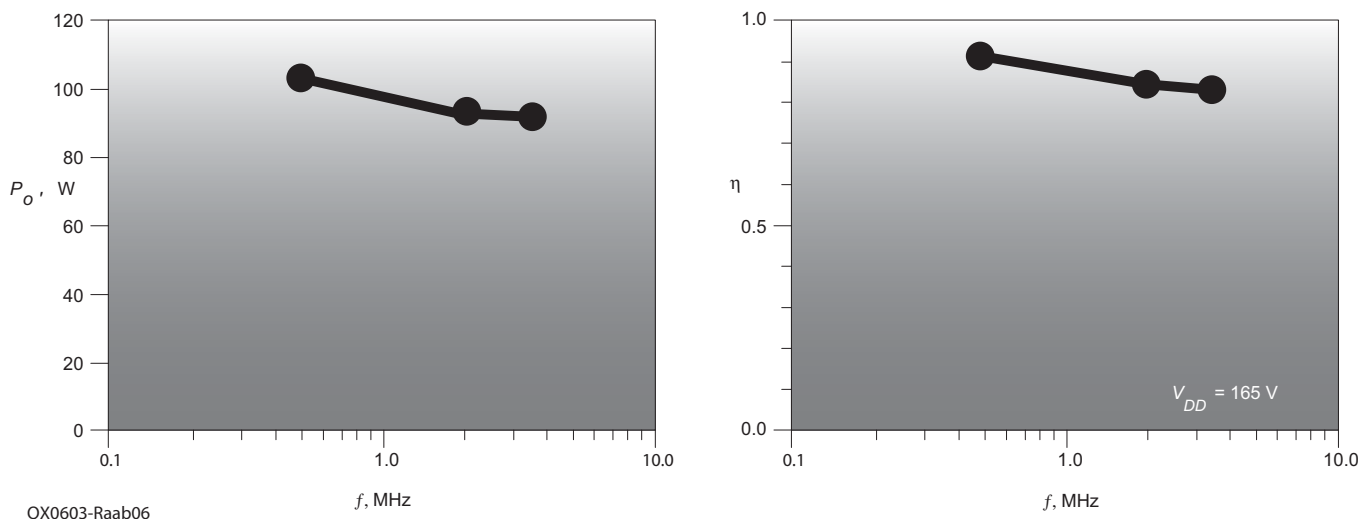


Figure 6 — Output and efficiency as functions of frequency.

specifying Q and determining R_{on} or by specifying R_{on} and determining Q .

In the previously presented design, the drain-load resistance is $50\ \Omega$, which is the same as the output resistance; hence, L1 and L2 are the same. Operation at higher power or from a lower V_{DD} may require transformation of the output resistance, hence different values of the inductors. Many different T networks can be designed that provide the desired drain-load resistance. For proper operation of the class-D amplifier, however, the reactance of L1 at the third harmonic must be at least nine times the drain-load resistance. Consequently, the reactance of L1 at the fundamental frequency must be three times the drain-load resistance. Generally, nothing is gained by making L1 larger than necessary, so its value should be the minimum that provides the desired transformation and the minimum harmonic impedance.

Recommendations

This amplifier was made by adapting an existing prototype. Consequently, the layout is somewhat of a kludge and not recommended. Improvements in the layout include:

- Elimination of about 2 inches between the driver and final;
- Installation of $1\text{-}\mu\text{F}$ chip capacitors right at the points to be bypassed;

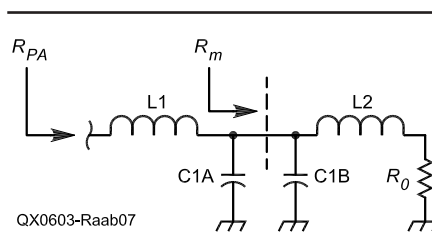


Figure 7 — T network viewed as back-to-back L networks.

- Shortening of all leads, and
- Elimination of the 3300-pF bypass capacitors.

A better layout and closer bypassing should allow operation from sinusoidal inputs of less amplitude. This can also be accomplished by placing a TTL line receiver to hard-limit the input before driving U101.

Note: A shorter version of this article appeared in the May/June 2005 issue of *The AMRAD Newsletter*.

Notes

¹H. L. Krauss, C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering*. New York: Wiley, 1980.

²F. H. Raab, "Switching transients in class-D RF power amplifiers," *Proc Seventh Int Conf HF Radio Syst and Techniques (HF'97)*, Nottingham, UK, pp 190-194, Jul 7-10, 1997.

³F. H. Raab, "Simple and inexpensive high-efficiency power amplifier for 160-40 meters," *Communications Quarterly*, vol 6, no. 1, pp 57-63, Winter 1996.

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